VMEbus™ FDDIXPress™ Board Installation Instructions

Document Number 108-7030-040

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FCC Warning

This equipment has been tested and found compliant with the limits for a Class A digital device, pursuant to Part 15 of the FCC rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

Attention

This product requires the use of external shielded cables in order to maintain compliance pursuant to Part 15 of the FCC Rules.

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Introduction

The FDDIXPress™ is a network connection product (adapter board and software) that provides high-speed fiber distributed data interface (FDDI) network connections. This manual provides instructions for installing the FDDIXPress board into a VMEbus™ option slot on the following Silicon Graphics® platforms:

- POWER Series™
- Professional Series
- IRIS Crimson™
- Onyx™ (deskside and rackmount)
- CHALLENGE L™ (also referred to as Challenge deskside)
- CHALLENGE XL™ (also referred to as Challenge rackmount)

The FDDIXPress board processes the transmission and reception of data packets (frames) across a 100-megabit-per-second FDDI network and maintains communication by wrapping in the event of a break in the ring (as illustrated in Figure In-1 and Figure In-2). The board is a single media access control (MAC) dual-attachment FDDI board; it can be connected as a dual-attachment station to the dual ring, as a single-attachment station to a concentrator, or as a dual-homed station, where both ports are attached to concentrators and one connection acts as a backup.

The FDDIXPress board for the above-listed platforms is a single-slot 6U board that resides in a 9U adapter board. The FDDIXPress is a VMEbus-compatible board that is based on a subset of the AMD SUPERNET™ LSI chips.

For a detailed description on the board, refer to Chapter 4, “Principles of Operation.”

Other FDDI Documents

There are a number of different FDDI products and documents that are available through Silicon Graphics. Some of these relate to the VMEbus version of the FDDIXPress and some do not. Table In-1 lists these different FDDI manuals and indicates if the manual is related to the VMEbus version of the FDDIXPress.

Table In-1 Other FDDI Documents

Document Number	Title	Related Document to VMEbus FDDIXPress?
008-1837-050	FDDIXPress 3.6 Release Notes	Yes
007-0813-050	FDDIXPress Administration Guide	Yes Note: See this guide for additional information on FDDI operation.
007-1588-020	FDDIXPress for IRIS Indigo Installation Guide	No
007-9046-010	Installing the FDDI Board, Personal IRIS	No
108-7028-010	FDDIXPress Board Installation Guide (for Magnum)	No
108-7038-010	FDDIXPress Controller Board Installation Instructions	No Note: This manual is not currently available.
007-2224-001	FDDIXPress for Indy Installation	No
007-2144-001	FDDIXPress Administration Guide for Indigo2 and Challenge M	No

Overview of FDDIXPress Board

This section describes the main features of the FDDIXPress board. The bulleted list points out the most important features of the board. Table In-1 highlights some of the specifications of the FDDIXPress controller board.

- Intelligent VMEbus FDDI node controller, based on a subset of the AMD SUPERNET LSI chips. See Chapter 4, “Principles of Operation” for more information.
- Custom buffer memory control.
- VMEbus data transfer capable of up to 40 MB per second.
- Support for DMA half-word aligned longword transfers.
- Dual attachment board, single MAC (DAS-SM). It supports the following attachment schemes: connected to the dual-ring as a dual-attached station, connected to a single concentrator to perform as a single-attached station (SAS), or connected to two different concentrator ports. (The latter scheme is known as “dual-homed”; one concentrator connection provides “backup” while the other carries data.)
- Optionally, support for an external optical bypass switch.

Table In-2 Board Specifications

Specifications	Value
Mechanical	Single high 6U VMEbus board that is mounted in a 6U-to-9U converter board.
Maximum number of boards per system	Four
Power	7.2 Amps of +5 VDC and 1.0 Amp of 12 VDC at 25 C
Environmental	
Operating temperature	0 to 55° C
Operating humidity	0 to 90% (noncondensing)

FDDI Terminology

This section illustrates some of the more important FDDI terms and concepts. Figure In-1 illustrates an FDDI dual ring with a variety of types of stations: dual-attachment, single-attachment, dual-homed, and concentrators. Figure In-2 shows a how a ring wraps when there is a break.

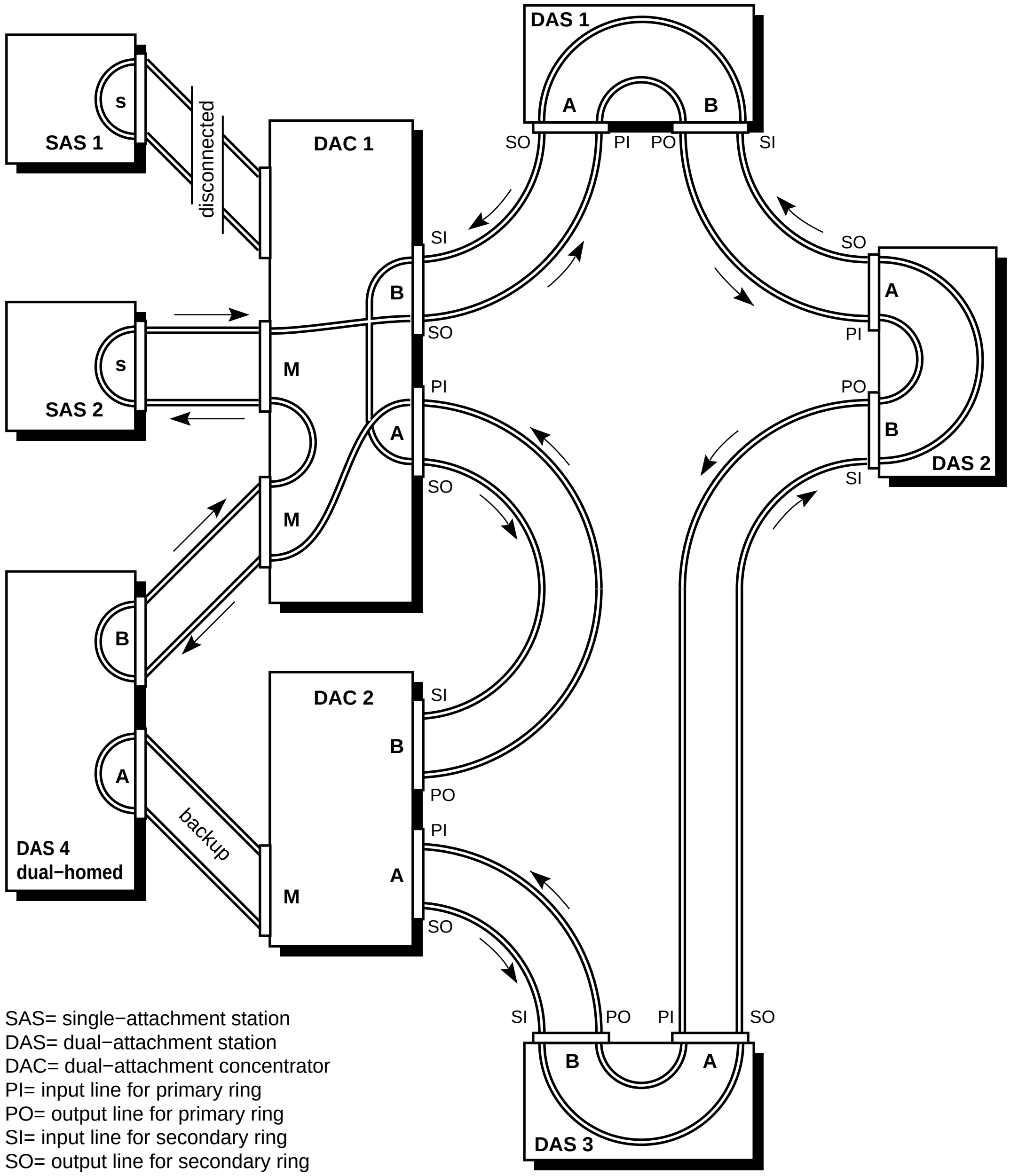
Figure In-1 FDDI Ring Topology: Normal Operation

Figure In-2 FDDI Ring Topology: Wrapped Ring Showing Fault Domain

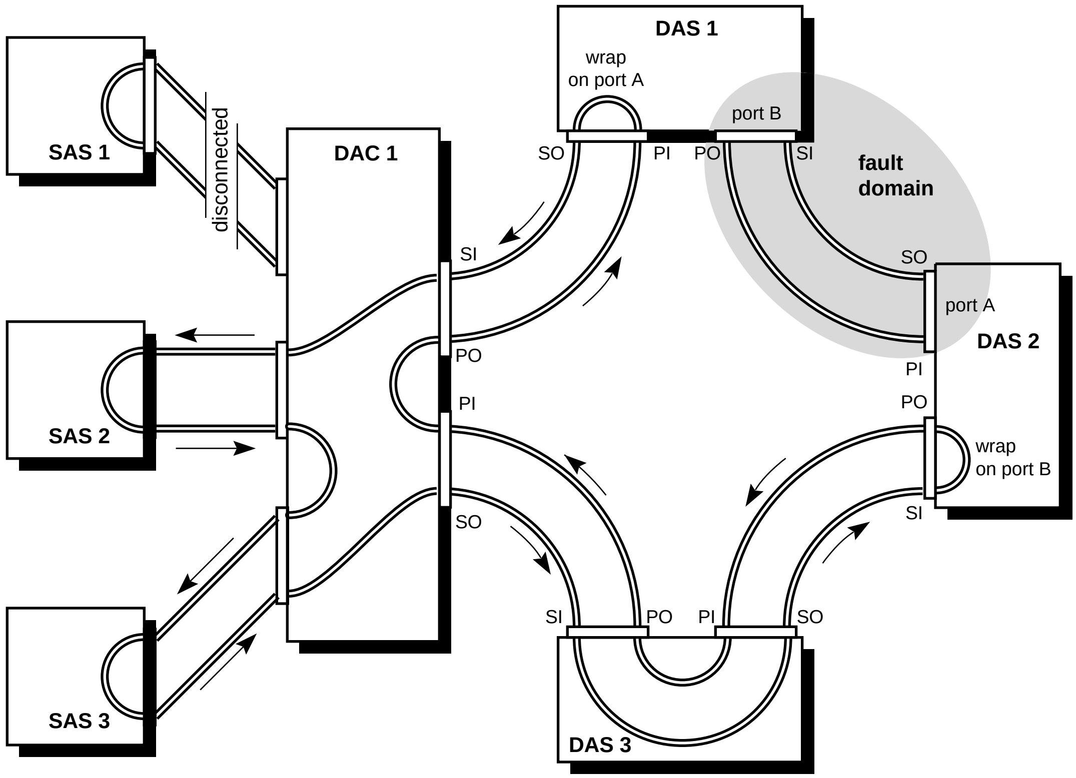
The break that is causing the fault domain illustrated in Figure In-2 could be a dysfunction of any of the following:

- the cable lying between DAS1 and DAS2
- the output connector for the primary ring (PO, one line of port B) at DAS1
- the input connector for the primary ring (PI, one line of port A) at DAS2
- a component on the adapter board for transmitting at DAS1 or for receiving at DAS2 on the primary ring

Notice that a powered-off or dysfunctional SAS (illustrated by SAS1 in both Figure In-1 and Figure In-2) does not cause the ring to wrap.



SAS= single−attachment station
DAS= dual−attachment station
DAC= dual−attachment concentrator
PI= input line for primary ring
PO= output line for primary ring
SI= input line for secondary ring
SO= output line for secondary ring



SAS= single−attachment station
DAS= dual−attachment station
DAC= dual−attachment concentrator
PI= input line for primary ring
PO= output line for primary ring
SI= input line for secondary ring
SO= output line for secondary ring

Chapter 1

Connectors, Jumpers, and Status Indicators

This chapter discusses important connectors, jumpers, and status indicators on the FDDIXPress board. For additional discussion on the FDDIXPress board hardware, refer to Chapter 4, “Principles of Operation.”

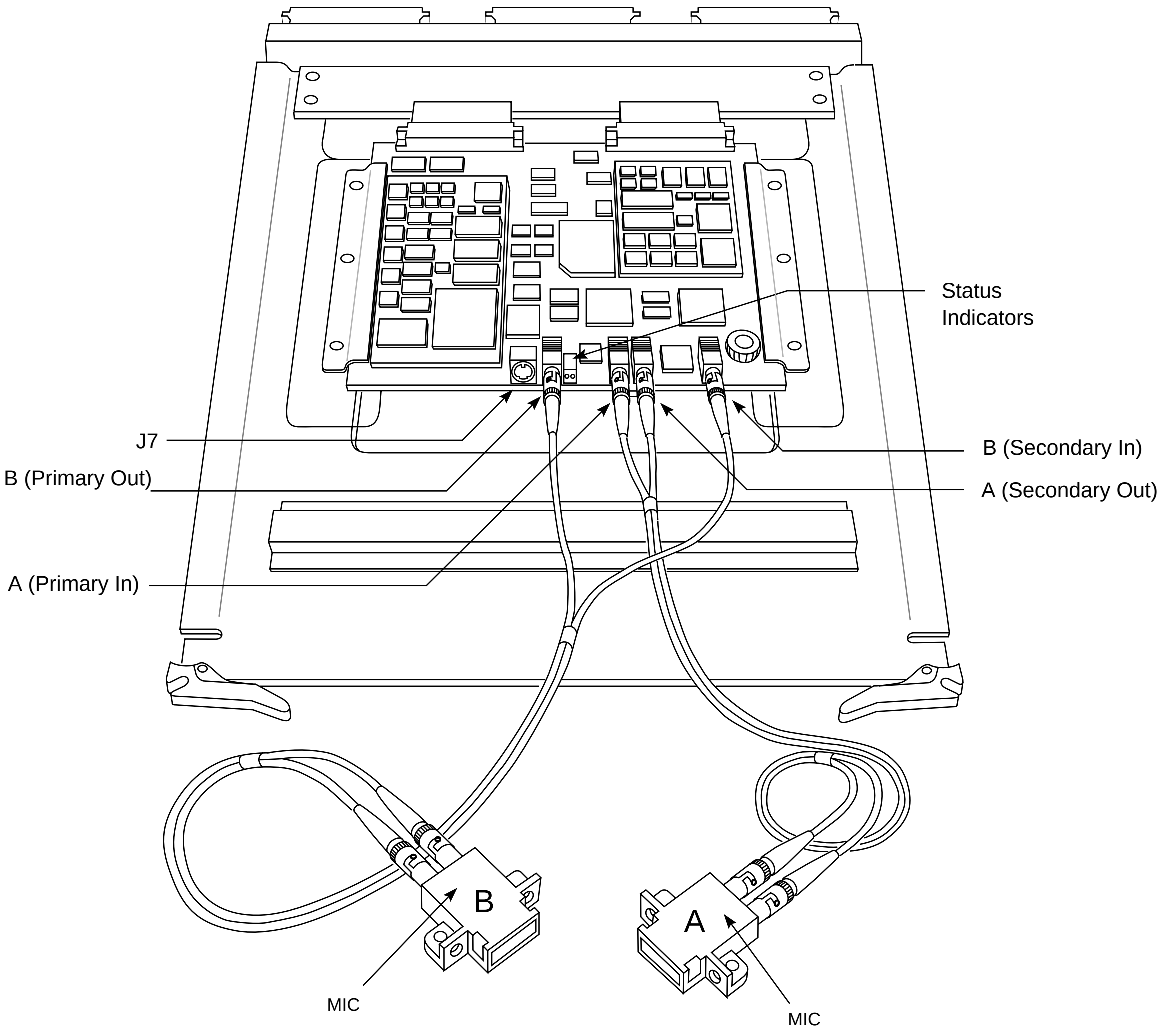
1.1 Connectors

Table 1-1 describes the most important connectors on the board. Figure 1-1 shows their locations.

Table 1-1 Connector Descriptions

Connector Name	Function
P1 and P2	Provides interface to the VMEbus.
A	Provides connection to fiber optic cable **A**. (For a dual-attached station, the cable consists of the primary ring input and secondary ring output.)
B	Provides connection to fiber optic cable **B**. (For a dual-attached station, the cable consists of primary ring output and secondary ring input.)
J3 (not used)	Serves as input connector to second FDDI controller board in dual MAC configuration.
J4 (not used)	Serves as output connector to second FDDI controller board in dual MAC configuration.
J7	Provides control line to optical bypass switch (OBS).

Figure 1-1 FDDIXPress Board’s Cable Connectors



1.2 Jumpers

Table 1-2 summarizes the jumper blocks on the FDDIXPress motherboard. Figure 1-2 illustrates the jumper block locations and default settings.

Table 1-2 Jumpers on Main Board

Jumper	Default Setting	Instruction	Description
JA1	Jumper	Do not alter default.	No jumper = single PHY. When jumper is installed, the board supports dual PHY configuration.

Table 1-2 (continued) Jumpers on Main Board

Jumper	Default Setting	Instruction	Description
JA2	Not applicable	Not used.	Not interpreted.
JA3	No jumper	Do not alter default.	No jumper = single-MAC. When jumper is installed, enables byte clock (BCLK) termination for dual-MAC boards.
JA4	No jumper	Do not alter default.	No jumper = single-MAC. When jumper is installed, disables local clock for dual-MAC boards.
JA5	No jumper	Do not alter default.	No jumper = host control of OBS. When jumper is installed, host cannot control optical bypass switch (OBS) for primary PHY.
JA6	No jumper	Do not alter default.	No jumper = host control of OBS. When jumper is installed, host cannot control optical bypass switch for secondary PHY.
JA7	Jumper	Do not alter default.	No jumper = early release (release at start of last BBSY cycle). When jumper is installed, VMEbus BBSY signal is released after the last cycle is completed.
JA8 to JA10	Level 0	Alteration optional.	Sets VMEbus request priority level. Can be set to 0 (lowest), 1, 2, or 3. See Figure 1-4 for details.
JA11	Unit 0	Must be changed when multiple boards are installed in one system.	Sets unit number for the board. Can be set to 0, 1, 2, or 3. See Figure 1-3 for details. Each FDDIXPress board in a system must have a unique unit number.
JA12	No jumper	Do not alter default.	Must not be jumpered.
J13	Jumper (pins 2 to 3)	Do not alter default.	When jumper is installed on pins 1-2, interrupt is generated when a frame is missed. When jumper is installed on pins 2-3, interrupt is not generated.
J14	Jumper (pins 2 to 3)	Do not alter default.	When jumper is installed on pins 1-2, enables frame segmentation into 2 KB segments. When jumper is over pins 2-3, disables frame segmentation.
J15	No jumper	Do not alter default.	No jumper = no interrupt when restricted token is received. When jumper is installed, enables restricted token interrupts.

Table 1-2 (continued) Jumpers on Main Board

Jumper	Default Setting	Instruction	Description
Note: Connectors J3 and J4 are not used. See Table 1-1 for more information.			

Jumper block **JA11** sets the unit number for the board. Each FDDIXPress board in a system must have a unique number; two or more FDDIXPress boards with the same unit number will cause the system to function in an unpredictable manner. When a single FDDIXPress board is installed in a system, the default setting for unit 0 should be used. When two or more FDDIXPress boards are installed in a system, set the **JA11** jumper on each board (as illustrated in Figure 1-3) so that the unit number is unique.

Up to four FDDIXPress boards can be used in each Challenge, Onyx, IRIS Crimson, Professional, or POWER Series workstation or server. The FDDIXPress boards in a system (unit 0, unit 1, unit 2, unit 3, as set by jumper block **JA11**) are controlled by drivers with similarly numbered interface names (*ipg0*, *ipg1*, *ipg2*, and *ipg3*). All FDDIXPress boards shipped from Silicon Graphics are configured as unit 0.

Note: See Section 1.4, "VMEbus Arbitration," regarding the arbitration scheme for single or multiple FDDIXPress board configurations.

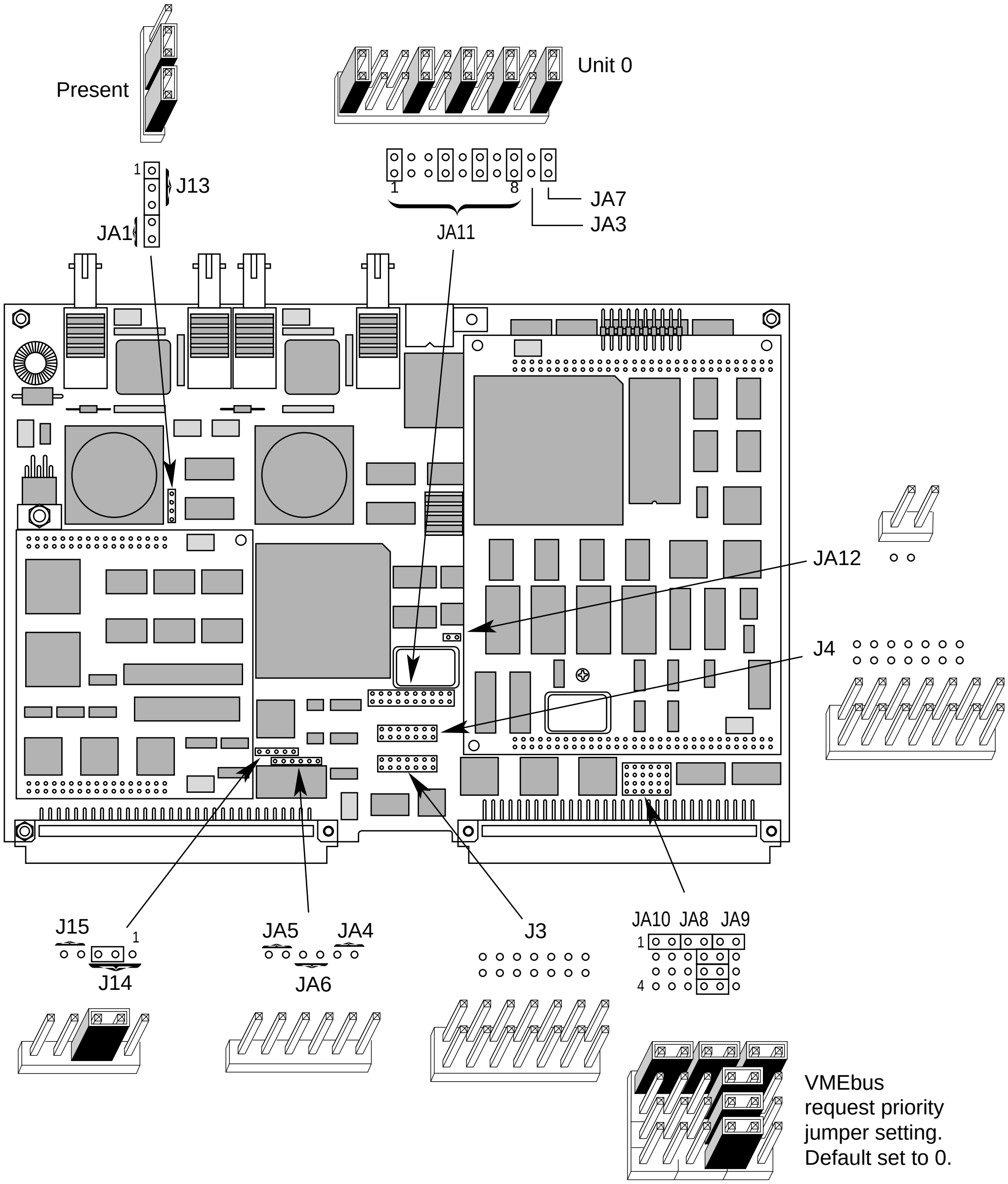


Figure 1-2 FDDIXPress Default Jumpers

Note: The request priority default setting of “0” applies to all Silicon Graphics systems with a VME bus such as the Challenge, Onyx, and POWER Series systems. See also Section 1.4, “VMEbus Arbitration,” for bus arbitration information.

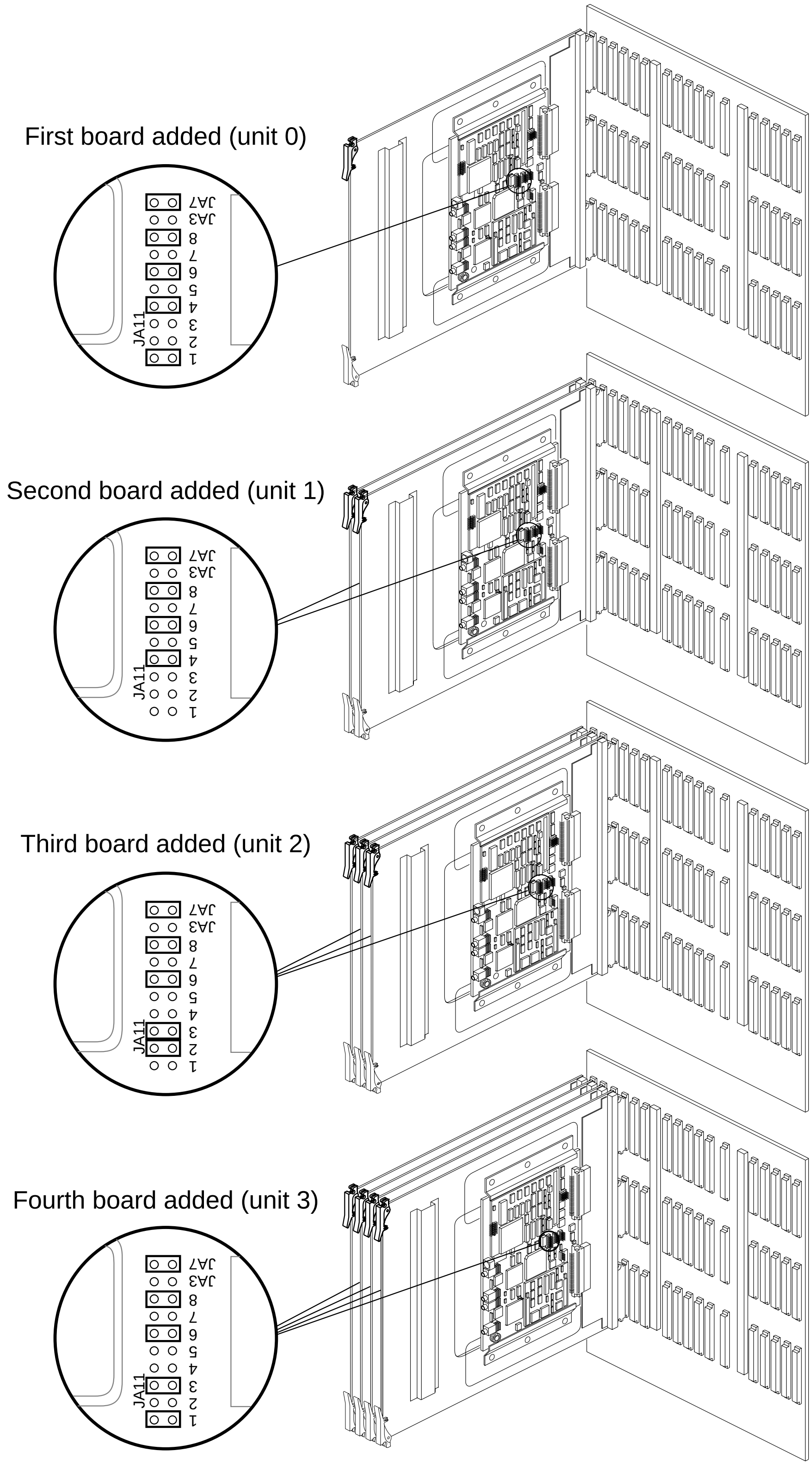


Figure 1-3 JA11 Jumper Settings for Multiple Board Installations

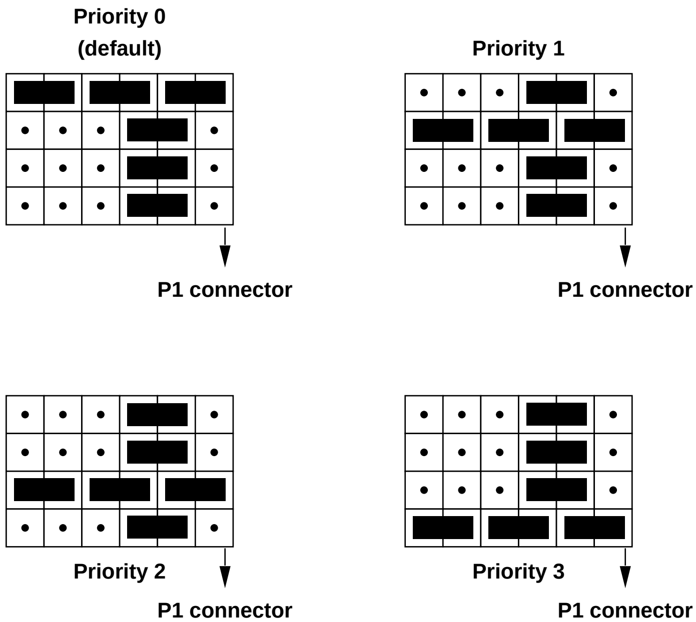


Figure 1-4 JA8-JA10 Jumper Settings for VMEbus Request Priority

1.3 LED Status Indicators

Table 1-3 describes the status indicators. Refer to Figure 1-1 for the locations of the LED status indicators.

Table 1-3 LED Status Indicators

LED Color	Status
Red is on; green is off.	FDDI ring is down.
Green is on; red is off.	FDDI board is operating, but network is quiet.
Both red and green are on.	FDDI ring is up and the board is active.

1.4 VMEbus Arbitration

The VME bus has four bus request levels (BR3 through BR0) and supports three arbitration schemes.

prioritized If more than one bus request is in the queue, the arbitration logic automatically grants bus access to the highest-level request first.

round-robin If no priority request is present, the arbitration logic grants bus access on a daisy-chained basis, with VME boards closest to the left side of the card cage (as you face the system) receiving access first. For example, if a VME board resides in slot 5 and another resides in slot 8, the VME board in slot 5 receives bus access before the board in slot 8. Slot 5 is closer the left side of the card cage.

single level If all the requests are at the same level (BR3 through BR0), the requests are daisy-chained.

In addition, the VME subsystem adheres to the following criteria:

- VME bus request level 3 is always higher priority than 0, 1, and 2.
- VME bus request levels 0, 1, and 2 are round robin.

Chapter 2

Installing FDDIXPress

This chapter describes how to install the FDDIXPress controller board into a Silicon Graphics system. A separate section is dedicated to each platform.

Caution: This product is not customer installable.

Installation of this product requires specific training and technical knowledge. These instructions have been provided for use by Silicon Graphics, Inc., System Support Engineers or other Silicon Graphics trained personnel only. This installation requires the installer to handle internal electrical power that is hazardous if the equipment is improperly disassembled or reassembled.

2.1 Installation Procedure for POWER Series and Professional Series

This section describes the steps for installing FDDIXPress into a POWER Series or Professional Series workstation or server. A maximum of four FDDIXPress boards can be installed into these systems.

Note: If you are installing the FDDIXPress board into the VMEbus-B of a Predator 3 (R2-4D POWER Center), you must have FDDIXPress 2.0 (or higher) and IRIX 4.0.1 or higher since this configuration is not supported in the earlier release.

2.1.1 Prepare for Installation

1. Verify that the system's operating system version (IRIX or *eoe1*) matches the version of FDDIXPress that you are going to install. Software compatibility information is located in the *FDDIXPress Release Notes*. If necessary, upgrade the operating system.
2. Once the system is ready to install FDDIXPress, perform a system backup and verify the saved files.

2.1.2 Install and Configure Software

1. Use this command to check if the FDDIXPress software has been installed:

```
% /usr/sbin/versions FDDIXPress
I FDDIXPress 03/02/93 FDDIXPress 3.1 Option
```

If the software is installed and the version is correct, proceed to the next step.

If the message `Nothing satisfies the selection criteria` is displayed or if the version is not correct, install FDDIXPress software using the IRIX installation method and the Inst commands **`install FDDIXPress`** and **`go`**.

2. Configure the FDDI network interface, as explained in the *FDDIXPress Release Notes* or in Chapter 2 of the *FDDIXPress Administration Guide.*

2.1.3 Configure the Board

1. If installing more than one FDDIXPress board, verify that each board's **JA11** jumper is set to a unique unit number. Refer to Figure 1-2 for details.
2. Attach the board's cables (1 optical bypass switch cable and two fiber optic cables) to the board.

   Each of the two fiber optic cables has a pair of ST™ connectors (each marked with an arrow indicating the direction of its signal). The ST connectors must be attached as illustrated in Figure 1-1, making sure to match cable **A** to the board's port A receptacles and cable **B** to the board's port B receptacles.

   Caution: If the ST connectors are not connected properly, the FDDI connection will not work.

   Attach the optical bypass switch cable to the board and to the panel plate, as illustrated in Figure 2-2.

2.1.4 Install the Hardware

Caution: The components are extremely sensitive to ESD (electrostatic discharge). Use proper antistatic procedures while handling all components.

1. Shut down the system according to the operating system instructions.
2. Turn off the power switch and unplug the power cable.
3. Remove the keyboard, Ethernet, SMD, ESDI, monitor or RGB cables, and any other cables from the I/O door.
4. Open the I/O door on your system.

   Caution: On a Twin Tower (POWER Station system) remove the bottom screw located on the I/O door between the hinges. If you do not remove this screw, the sheet metal could be damaged during disassembly.

5. Select a VMEbus slot for the FDDIXPress board. It is recommended that you select the first available VMEbus slot. (If you leave any VMEbus slots empty, you must jumper them as explained in Section 2.1.5.1, "Backplane Considerations.") Refer to Table 2-1 through Table 2-6 to help determine the proper slot.
6. Install the FDDIXPress board and extender board into the VMEbus slot. See Figure 2-1 for an example of installing an FDDIXPress board into a system.
7. Attach the two mounting panel plates to two different openings in the I/O panel door.

8. Finish the installation by following the instructions in Section 2.5, “Completing Board Installation.”

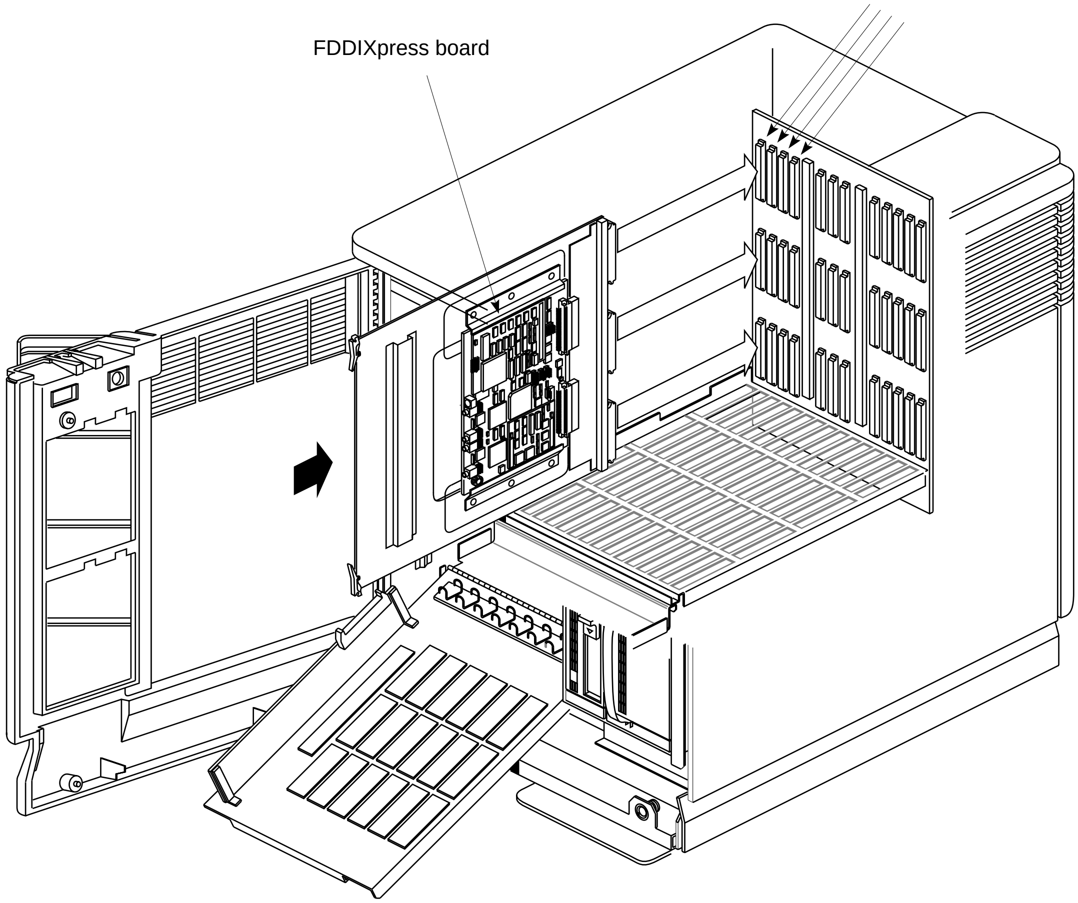


Figure 2-1 Installing the Board

Table 2-1 Professional Series or Omni IRIS-4D / 85GT(Diehard1) VMEbus Slot Allocations

Slot	IRIS-4D 60G 12-Slot Multi-Board Computer (MBC)	IRIS-4D 7/80 GT 12-Slot Single-Board Computer (SBC)	IRIS 4-D 85GT 13-Slot Chassis
1	CPU board only	CPU board only	CPU board only
2	FPP board only	Memory board (pre-empted VMEbus slot)	Memory board (or optional VMEbus board)
3	Memory board only	Memory board (pre-empted VMEbus slot)	Memory board (or optional VMEbus board)
4	Memory board only	ESDI Controller board (pre-empted VMEbus slot)	ESDI Controller board

Table 2-1 Professional Series or Omni IRIS-4D / 85GT(Diehard1) VMEbus Slot Allocations

Slot	IRIS-4D 60G 12-Slot Multi-Board Computer (MBC)	IRIS-4D 7/80 GT 12-Slot Single-Board Computer (SBC)	IRIS 4-D 85GT 13-Slot Chassis
5	Memory board only	CMC Ethernet Controller (pre-empted VMEbus slot)	CMC Ethernet Controller
6	Optional VMEbus board	ISI tape controller (or optional VMEbus board)	ISI tape controller (or optional VMEbus board)
7	Optional VMEbus board	Optional VMEbus board	Optional VMEbus board
8	Optional VMEbus board	GE4	GE4
9	Optional VMEbus board	GM1	GM1
10	GF3	RM1	RM1
11	DE3	RV1	RM1
12	TB2	RM1	RV1.5
13	N / A	N / A	Optional Video Board (for example VP1)

Note: The Omni IRIS-4D / 85GT backplane adheres to the same practice as prior Silicon Graphics backplanes. All unused slots must have jumpers H71, HUB3, H7B2, H7B1 and H7BG pinned.

Table 2-2 Single Tower (Diehard II) VMEbus Slot Allocations

Slot Number	Slot Type
1	Optional VMEbus board
2	Optional VMEbus board
3	Optional VMEbus board
4	Optional VMEbus board
5	I / O board
6	CPU board
7	Optional CPU board
8	MC2 board
9	GM board
10	GE board
11	RM board
12	RM board
13	DG1 board

Table 2-2 (continued) Single Tower (Diehard II) VMEbus Slot Allocations

Slot Number	Slot Type
14	Optional video board

Table 2-3 Twin Tower VMEbus Slot Allocations

Slot Number	Slot Type
1	Optional VMEbus board
2	Optional VMEbus board
3	Optional VMEbus board
4	Optional VMEbus board
5	I/O board
6	CPU board
7	Optional CPU board
8	MC2 board
9	MC2 board
10	GM board
11	GE board
12	RM board
13	Optional RM board
14	DG1 board
15	Optional video board

Table 2-4 POWER Center (Predator) VMEbus Slot Allocations

Slot Number	Slot Type
1	Optional VMEbus board
2	Optional VMEbus board
3	Optional VMEbus board
4	Optional VMEbus board
5	Optional VMEbus board
6	Optional VMEbus board
7	I/O board

Table 2-4 POWER Center (Predator) VMEbus Slot Allocations

Slot Number	Slot Type
8	1st CPU board
9	2nd CPU board (if applicable)
10	3rd CPU board (if applicable)
11	4th CPU board (if applicable)
12	MC2 board
13	MC2 board
14	GM board
15	GE board
16	RM board
17	Optional RM board
18	DG1 board
19	Optional video board

Table 2-5 R2-4D POWER Center (Predator 3) VMEbus Slot Allocations

Slot Number	Slot Type
1	Optional VMEbus-A board
2	Optional VMEbus-A board
3	Optional VMEbus-A board
4	Optional VMEbus-A board
5	Optional VMEbus-A board
6	Optional VMEbus-A board
7	1st IO3 board
8	1st CPU board
9	2nd CPU board (if applicable)
10	3rd CPU board (if applicable)
11	4th CPU board (if applicable)
12	1st MC2 board
13	2nd MC2 board (if applicable)
14	2nd IO3 board
15	Optional VMEbus-B board

Table 2-5 R2-4D POWER Center (Predator 3) VMEbus Slot Allocations

Slot Number	Slot Type
16	Optional VMEbus-B board
17	Optional VMEbus-B board
18	Optional VMEbus-B board
19	Optional VMEbus-B board

Table 2-6 SkyWriter VMEbus Slot Allocations

Slot Number	Board
1	Optional VMEbus board
2	Optional VMEbus board
3	Optional VMEbus board
4	Optional VMEbus board
5	Pipeline 1 optional video board
6	Pipeline 1 DG1 board (optional EV1 board)
7	Pipeline 1 RM3 board
8	Pipeline 1 RM3 board
9	Pipeline 1 GE6 board
10	Pipeline 1 GM3 board
11	IO2 or IO3 board
12	IP board
13	IP board
14	MC2 board
15	Pipeline 0 GM3 board
16	Pipeline 0 GE6 board
17	Pipeline 0 RM3 board
18	Pipeline 0 RM3 board
19	Pipeline 0 DG1 board with VX1 board
20	Pipeline 0 Optional video board

2.1.5 Other Information

This section contains information about special installations such as backplane considerations when you skip a VMEbus slot, configuration instructions when you install into a second card cage, and information specific for a particular platform.

2.1.5.1 Backplane Considerations

After you have inserted the FDDI board into an empty VMEbus slot, you may need to add jumpers to the backplane. You may also need to reconfigure the */usr/sysgen/system* file if you are installing the board into the VMEbus B channel (indicated as VMEbus-B) of a dual VMEbus R2-4D rackmount chassis.

When the POWER Series IRIS-4D boots after power-on, it probes its I/O channels to identify the hardware that is plugged into each VMEbus slot. The power-up sequence probes each VMEbus slot sequentially until reaching the last used slot in each I/O channel. It must find either a VMEbus I/O controller or jumpers in each VMEbus slot location. If the slots aren't properly jumpered, the workstation or server will hang before booting or never enable the new hardware.

Whether or not you need to add jumpers to the backplane is determined by two factors:

- the VMEbus slot chosen
- the backplane of the workstation or server

You need to reconfigure the */usr/sysgen/system* file only if you are installing the FDDI board into the VMEbus-B channel of a dual VMEbus R2-4D rackmount chassis.

When you are adding VMEbus boards into several chassis, keep the following general rules in mind:

1. For the IRIS-4D Professional Series (which includes the IRIS-4D 60, 70, 80, and 85 models), remove the existing VMEbus backplane jumpers from the slot when you add a VMEbus board. All unused slots must be jumpered.
2. For the IRIS-4D POWER Series (IRIS 120/GTX and later), add the VMEbus board into the first available VMEbus in numerical sequence without leaving any gaps. Jumpering the unused slots is unnecessary. However, if VMEbus boards are added out of numerical sequence leaving gaps, you must add jumpers to the slots that were skipped.
3. For the R2-4D dual VMEbus model 19-slot rackmount chassis, the */usr/sysgen/system* file must be reconfigured for new VMEbus boards.

There is no prescribed sequence of VMEbus boards that is necessary. In the past, SSEs were advised to add disk controllers first, then add Ethernet controllers second. These sequences were designed for consistency, not electronic necessity. All VMEbus boards are serviced by the backplane according to the board's priority interrupt level, not by the slot order.

Note: If you need to skip a slot to fit oversized VMEbus boards or to improve airflow in a chassis, make sure that you jumper only the slots corresponding to empty slots; don't jumper slots that actually house VMEbus boards!

2.1.5.2 Configuring a Dual VMEbus R2-4D POWER Center

When a R2-4D system is configured with dual IO3s, the VMEbus boards can be added either to the VME bus A or to VMEbus B. Add the VMEbus boards into the lowest slot number for each of VMEbus-A and VMEbus-B. See Table 3-5. As Table 3-5 shows, slot 1 is the first slot location for VMEbus-A and slot 15 is the first slot location for VMEbus-B.

If you are adding FDDIXPress boards into the VMEbus-A (slots 1-6), you won't have to edit the system configuration file */usr/sysgen/system* file; the default settings allow you to add to up to four FDDIXPress boards into VMEbus-A. However, once you start adding FDDIXPress boards into VMEbus-B, the base and probe values in the */usr/sysgen/system* must be edited to locate those devices on VMEbus-B. Once the file has been edited, a new kernel must be generated and booted. Information on how to do so is included in the comments in the */usr/sysgen/system file*, and a summary of this information as it applies to an FDDIXPress board installation follows.

The FDDIXPress board appears in the */usr/sysgen/system* file as `module=if_ipg`. The default entries for the FDDIXPress board cover four FDDIXPress boards on VMEbus-A. Each FDDIXPress board has a base VMEbus address specified by the lower 16 bits of supervisor space. These addresses are the same whether the FDDIXPress board is on VMEbus-A or VMEbus-B. These values are indicated in bold italicized text. The file presents the fourth FDDIXPress board first, and it is designated as `unit=3`. Truncated versions of the VMEbus-A entries (so that you can see what numbers remain the same) are shown below:

```
unit=3 base=0xB7C1B400 exprobe=(r, 0xB7C1B402,2,0xfdd1,0xffff)
unit=2 base=0xB7C1B200 exprobe=(r, 0xB7C1B202,2,0xfdd1,0xffff)
unit=1 base=0xB7C1AE00 exprobe=(r, 0xB7C1AE02,2,0xfdd1,0xffff)
unit=0 base=0xB7C1AC00 exprobe=(r, 0xB7C1AC02,2,0xfdd1,0xffff)
```

The lines shown above are for VMEbus-A FDDIXPress boards. To add an FDDIXPress board into VMEbus-B, the high order bits for the base and probe locations must be changed for each board added into the chassis. The changes are shown below in bold text:

```
unit=3 base=0xB781B400 exprobe=(r, 0xB781B402,2,0xfdd1,0xffff)
unit=2 base=0xB781B200 exprobe=(r, 0xB781B202,2,0xfdd1,0xffff)
unit=1 base=0xB781AE00 exprobe=(r, 0xB781AE02,2,0xfdd1,0xffff)
unit=0 base=0xB781AC00 exprobe=(r, 0xB781AC02,2,0xfdd1,0xffff)
```

Configuration Example

To add three FDDIXPress boards to a dual VMEbus R2 rackmount chassis, follow these steps:

1. After unpacking the FDDIXPress boards, check the **JA11** jumper on the first board to make sure that it has the correct jumper settings for the first board, shown in Figure 1-3 as unit 0.
2. Change the jumper settings on the second FDDIXPress board to the unit 1 settings, as shown in Figure 1-3.
3. Change the jumper settings on the third FDDIXPress board to the unit 2 settings, as shown in Figure 1-3.
4. Add unit 0 into slot 1.
5. Add unit 1 into slot 15.
6. Add unit 2 into slot 16.
7. Become superuser and open the */usr/sysgen/system* file under the *vi* screen editor.

   Caution: Always make a copy of files before making any line changes.
8. Locate the appropriate vector lines corresponding to the device (or board) name. Find this line for the unit 0 FDDI board:

   ```
   VECTOR: module=if_ipg vector=0xc7 ipl=4 unit=0 base=0xB7C1AC00
   exprobe=(r, 0xB7C1ACO2,2,0xfdd1,0xffff)
   ```

   Since the first board is going to be part of VMEbus-A bus, you don’t have to change this line.

9. The entries for unit=1 and unit =2 must be changed for VMEbus-B. In each of the unit=1 and unit=2 lines, replace the 0xB7C in the base address and probe address to 0xB78, as shown in bold italicized text:

```
VECTOR: module=if_ipg vector=0xc5 ipl=4 unit=2 base=0xB781B200
exprobe=(r, 0xB781B202,2,0xfdd1,0xffff)

VECTOR: module=if_ipg vector=0xcd ipl=4 unit=1 base=0xB781AE00
exprobe=(r, 0xB781AE02,2,0xfdd1,0xffff)

VECTOR: module=if_ipg vector=0xc7 ipl=4 unit=0 base=0xB7C1AE00
exprobe=(r, 0xB7C1AC02,2,0xfdd1,0xffff)
```

10. Save your changes and exit the file.
11. Reboot to rebuild the kernel.

    Note: When updating a kernel using Inst, a new */usr/sysgen/system* file is created with all base and interrupt addresses in the default (VMEbus-A) range. Before executing autoconfig to configure a new kernel, the relevant VMEbus-B addresses must be merged into */usr/sysgen/system* from */usr/sysgen/system 0*. If it is not, the operating system will not find any of the I/O devices on VMEbus-B when the system boots.

2.1.5.3 FDDI I/O Plate Assembly Connections

Caution: Remember, the fiber in the cable is made of glass and is therefore breakable. Do not overly bend, flex, or tug on a fiber cable.

1. Remove the plate coverings from two connector cutouts from the back of the I/O panel.

   Note: Two I/O panel connectors are used per FDDI board. For example, if you are installing two FDDI boards, you need four I/O panel slots.

2. Install the media interface connectors (MICs) into the exposed slots. See Figure 2-2.
3. Attach the fiber optic cables to the connectors on the FDDI board. Make sure that the direction of the arrow on each cable matches the connector and that cable A is connected to the board’s port A connectors and cable B is connected to the board’s port B connectors, as illustrated in Figure 1-1.
4. Attach the Optical Bypass Switch (OBS) to the board by following the instructions that accompanied the OBS.
5. Attach the other ends (the MICs) of each cable to the appropriate A and B panel plates.

2.1.5.4 Important POWER Center (Twin Tower) Installation Information

Because of the narrow distance between the PC board and the back of the I/O panel on the Twin Tower chassis, special I/O plate assembly installation is required. See Figure 2-3.

1. *Always* install the I/O plate assemblies in the left column panel slots. *Never* install the plate assemblies in the right column in the top two slots.
2. If possible, place the plate assemblies in the top two slots.

3. Ensure that the fiber optic cables are attached to the A and B connectors on the FDDI board. Make sure that the direction of the arrows on the cable match up with the connector. In addition, ensure that the Optical Bypass Switch cable is attached. See Figure 2-2.

   Caution: The FDDI connector and cable may push against the front of the PC boards; be careful when closing the I/O panel after installation.

4. Close the panel carefully to see if the FDDI connector and cables come in contact with the front edge of the PC boards. See Figure 2-3. Ensure that the connector and cables do not pinch against the boards.

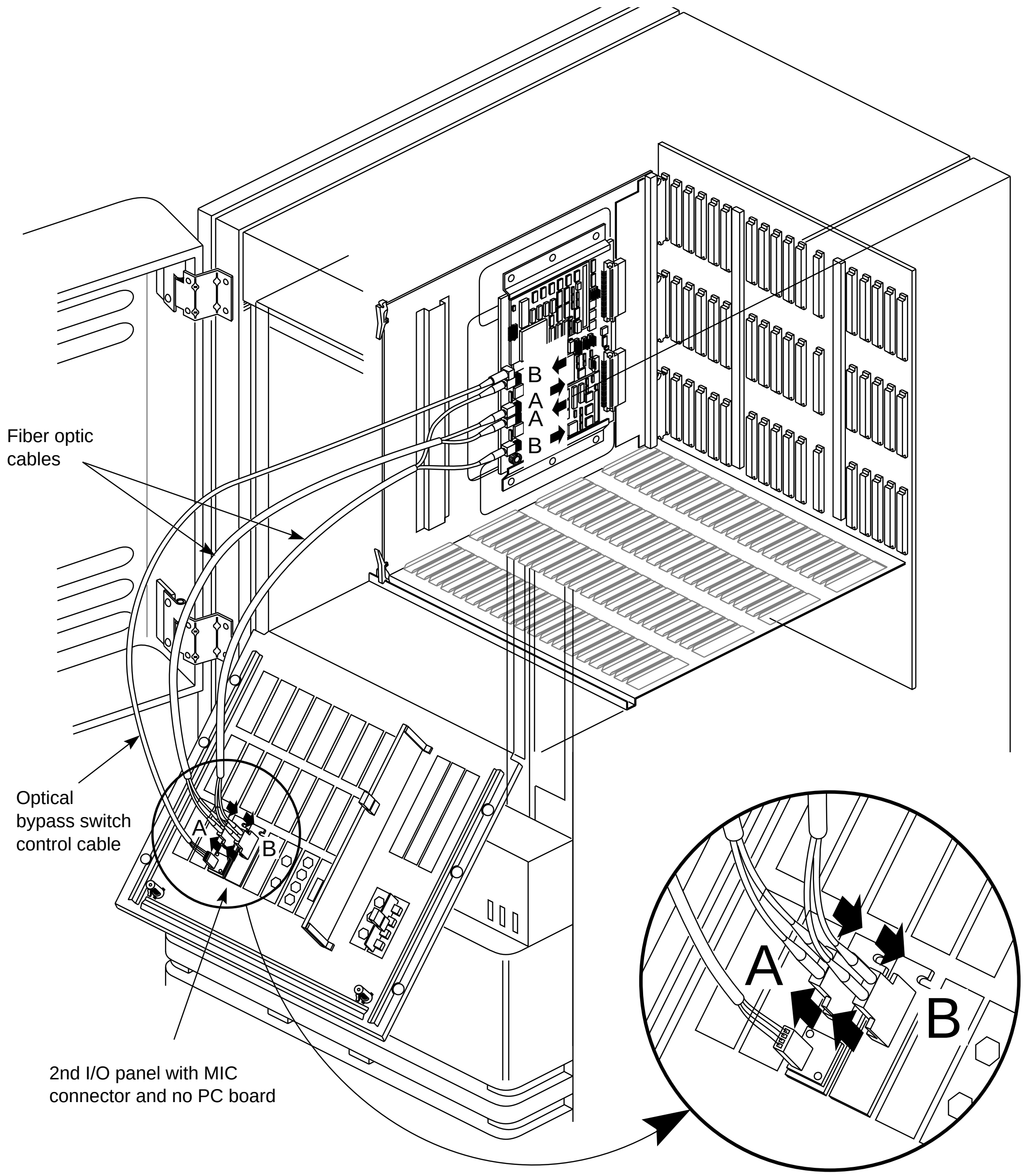


Figure 2-2 Internal Connections for FDDIXPress

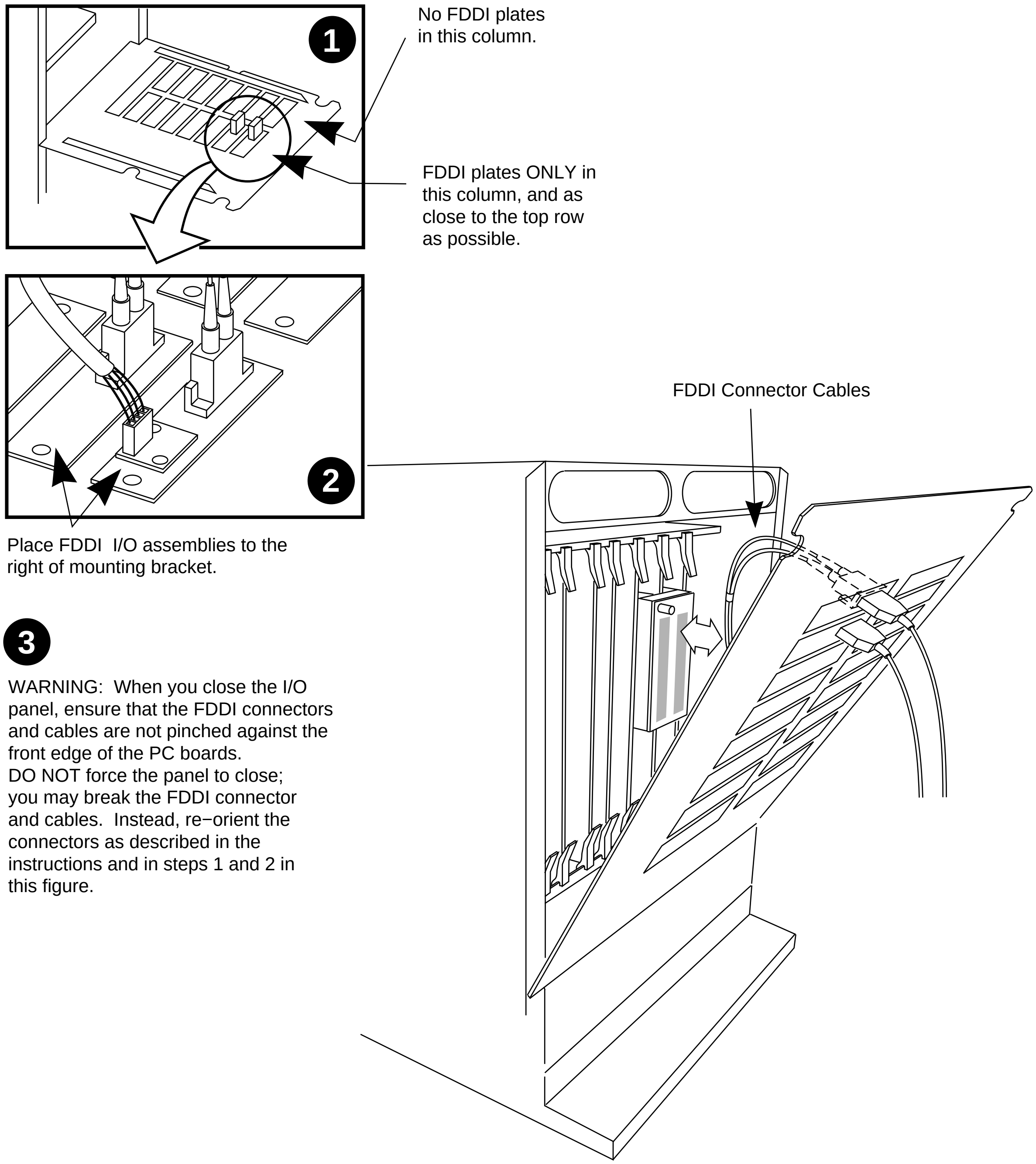


Figure 2-3 POWER Station (Twin Tower) Connections

2.2 Installation Procedure for IRIS Crimson

This section describes the steps for installing FDDIXPress into an IRIS Crimson workstation or server. A maximum of four FDDIXPress boards can be installed into a Crimson system.

2.2.1 Prepare for Installation

1. Verify that the system's operating system version (IRIX or *eoe1*) version matches the version of FDDIXPress that you are going to install. Software compatibility information is located in the *FDDIXPress Release Notes*. If necessary, upgrade the operating system.
2. Once the system is ready to install FDDIXPress, perform a system backup and verify the saved files.

2.2.2 Install and Configure Software

1. Use this command to check if the FDDIXPress software has been installed:

   ```
   % /usr/sbin/versions FDDIXPress
   I   FDDIXPress   date   FDDIXPress version Option
   ```

   If the software is installed and the version is correct, proceed to the next step.

   If the message `Nothing satisfies the selection criteria` is displayed or if the version is not correct, install FDDIXPress software using the IRIX installation method and the Inst commands **install FDDIXPress** and **go**.
2. Configure the FDDI network interface, as explained in the *FDDIXPress Release Notes* or in Chapter 2 of the *FDDIXPress Administration Guide*.

2.2.3 Configure the Board

1. If installing more than one FDDIXPress board, verify that each board's **JA11** jumper is set to a unique unit number. Refer to Figure 1-2 for details.
2. Attach the board's cables (1 optical bypass switch cable and two fiber optic cables) to the board.

   Each of the two fiber optic cables has a pair of ST connectors (each marked with an arrow indicating the direction of its signal). The ST connectors must be attached as illustrated in Figure 1-1, making sure to match cable **A** to the board's port A receptacles and cable **B** to the board's port B receptacles.

   Caution: If the ST connectors are not connected properly, the FDDI connection will not work.

   Attach the optical bypass switch cable to the board and to the panel plate, as illustrated in Figure 2-2.

2.2.4 Install the Hardware

1. Shut down the system according to the operating system instructions.
2. Turn off the power switch and unplug the power cable.
3. Remove the keyboard, Ethernet, SMD, ESDI, monitor, or RGB cables, and any other cables from the I/O door.
4. Open the I/O door on your system.

   Caution: The components are extremely sensitive to ESD (electrostatic discharge). Use proper antistatic procedures while handling all components.

5. Select a VMEbus slot for the FDDIXPress board. It is recommended that you select the first available VMEbus slot. (If you leave any VMEbus slots empty, you must jumper them as explained in Section 2.1.5.1, "Backplane Considerations.")
6. Install the FDDIXPress board and extender board into the VMEbus slot. See Figure 2-1 for an example of installing an FDDIXPress board into a system.
7. Attach the two panel plates to two different openings in the I/O panel door.
8. Finish the installation by following the instructions in Section 2.5, "Completing Board Installation."

2.3 Installation Procedure for Challenge L and XL

This section describes the steps for installing FDDIXPress into a Challenge L (also known as Challenge deskside) or Challenge XL (also known as Challenge rackmount) system. A maximum of four FDDIXPress boards can be installed into a Challenge system.

2.3.1 Prepare for Installation

1. Verify that the system's operating system version (IRIX or *eoe1*) matches the version of FDDIXPress that you are going to install. Software compatibility information is located in the *FDDIXPress Release Notes*. If necessary, upgrade the operating system.
2. Once the system is ready to install FDDIXPress, perform a system backup and verify the saved files.

2.3.2 Install and Configure Software

1. Use this command to verify that the FDDIXPress software has been installed:

   ```
   % /usr/sbin/versions FDDIXPress
   I   FDDIXPress   date   FDDIXPress version Option
   ```

   If the software is installed and the version is correct, proceed to the next step.

   If the message `Nothing satisfies the selection criteria` is displayed or if the version is not correct, install the FDDIXPress software, using the IRIX installation method and the Inst commands **install FDDIXPress** and **go**.

2. Configure the FDDI network interface, as explained in the *FDDIXPress Release Notes* or in Chapter 2 of the *FDDIXPress Administration Guide*.

2.3.3 Configure the Board

1. If installing more than one FDDIXPress board, verify that each board's **JA11** jumper is set to a unique unit number. Refer to Figure 1-2 for details.
2. Attach the board's cables (1 optical bypass switch cable and two FDDI cables) to the board.

   Each of the two FDDI cables has a pair of ST connectors (each marked with an arrow indicating the direction of its signal). The ST connectors must be attached as illustrated in Figure 1-1, making sure to match cable **A** to the board's port A receptacles and cable **B** to the board's port B receptacles.

   Caution: If the ST connectors are not connected properly, the FDDI connection will not work.

   Attach the optical bypass switch cable to the board, as illustrated in Figure 2-2.
3. Disconnect the MIC connectors (on the FDDI cables) from their previous panel plates (two). Then, attach both MICs to the new Challenge panel plate (only one). Be sure to match the MICs to the labels on the plate.
4. Attach the optical bypass switch cable to the new mounting plate.

2.3.4 Install the Hardware

1. Shut down the system according to the operating system instructions.
2. Turn off the power and unplug the power cable.
3. Remove all cables from the I/O door.
4. Open the I/O door on the system.

   Caution: The components are extremely sensitive to ESD (electrostatic discharge). Use proper antistatic procedures while handling all components.
5. Select a VMEbus slot for the FDDIXPress board. It is recommended that you use the first available VMEbus slot. For a Challenge L (deskside) system, see Table 2-7 and Figure 2-4 for additional information. For a Challenge XL (rackmount) system, see Table 2-8 and Figure 2-5.
6. Verify that a power supply board has been installed for the VMEbus slot(s) you have selected. On a Challenge L (deskside) system, VMEbus power supply boards are installed at the back of the system, on the other side of the VMEbus connectors. On a Challenge XL (rackmount) system, VMEbus power supply boards are installed in card cage 1.
7. Install the FDDIXPress board and extender board into the VMEbus slot. The side of the board with most of the components faces to your right, as illustrated in Figure 2-1.
8. If you decide not to use the first available VMEbus slot, follow the instructions in the system's installation instruction manual to jumper the empty slots.

9. Attach the panel plate to the I/O panel door.
10. Close the I/O door on the system.
11. Finish the installation following the instructions in Section 2.5, “Completing Board Installation.”

Table 2-7 Challenge L Board Slot Allocation

Slot Number	Board Type
1	Not to be used for VMEbus boards
2	Not to be used for VMEbus boards
3	Not to be used for VMEbus boards
4	Not to be used for VMEbus boards
5	Not to be used for VMEbus boards
6	IO4 and VCAM (VMEbus Channel Adapter Module)
7	First VMEbus Board
8	Second VMEbus Board
9	Third VMEbus Board
10	Fourth VMEbus Board
11	Fifth VMEbus Board

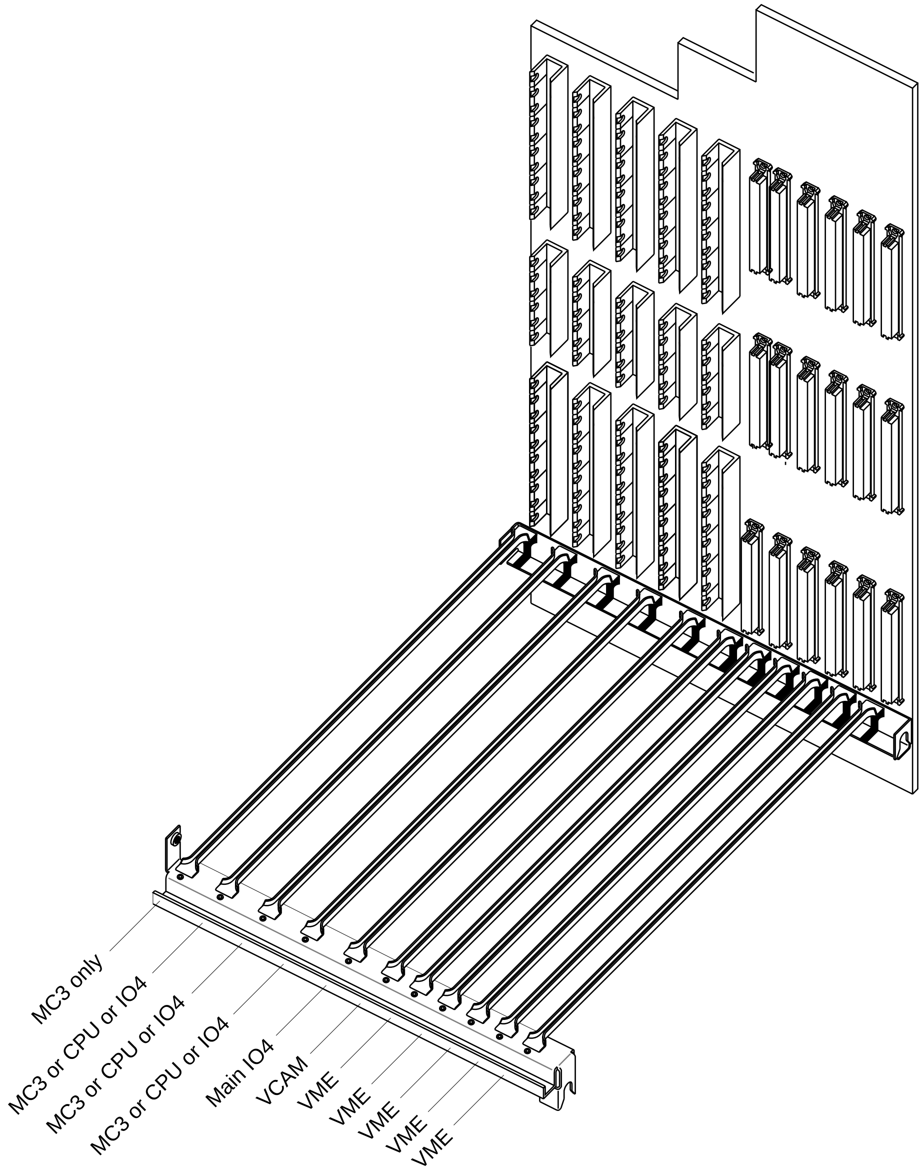


Figure 2-4 Challenge L Slot Locations

Table 2-8 Challenge XL Board Slot Allocations

Slot Number, Card Cage	Board Type
1, Card Cage 2	Not to be used for VMEbus boards
2, Card Cage 1	Not to be used for VMEbus boards
3, Card Cage 2	Not to be used for VMEbus boards
4, Card Cage 1	Not to be used for VMEbus boards

Table 2-8 Challenge XL Board Slot Allocations

Slot Number, Card Cage	Board Type
5, Card Cage 2	Not to be used for VMEbus boards
6, Card Cage 1	Not to be used for VMEbus boards
7, Card Cage 2	Not to be used for VMEbus boards
8, Card Cage 1	Not to be used for VMEbus boards
9, Card Cage 2	Not to be used for VMEbus boards
10, Card Cage 1	Not to be used for VMEbus boards
11, Card Cage 2	Not to be used for VMEbus boards
12, Card Cage 2	Not to be used for VMEbus boards
13, Card Cage 2	Not to be used for VMEbus boards
14, Card Cage 2	Not to be used for VMEbus boards
15, Card Cage 2	Main IO4
16, Card Cage 2	VCAM
17, Card Cage 2	First VMEbus board
18, Card Cage 2	Second VMEbus board
19, Card Cage 2	Third VMEbus board
20, Card Cage 2	Fourth VMEbus board
21, Card Cage 2	Fifth VMEbus board

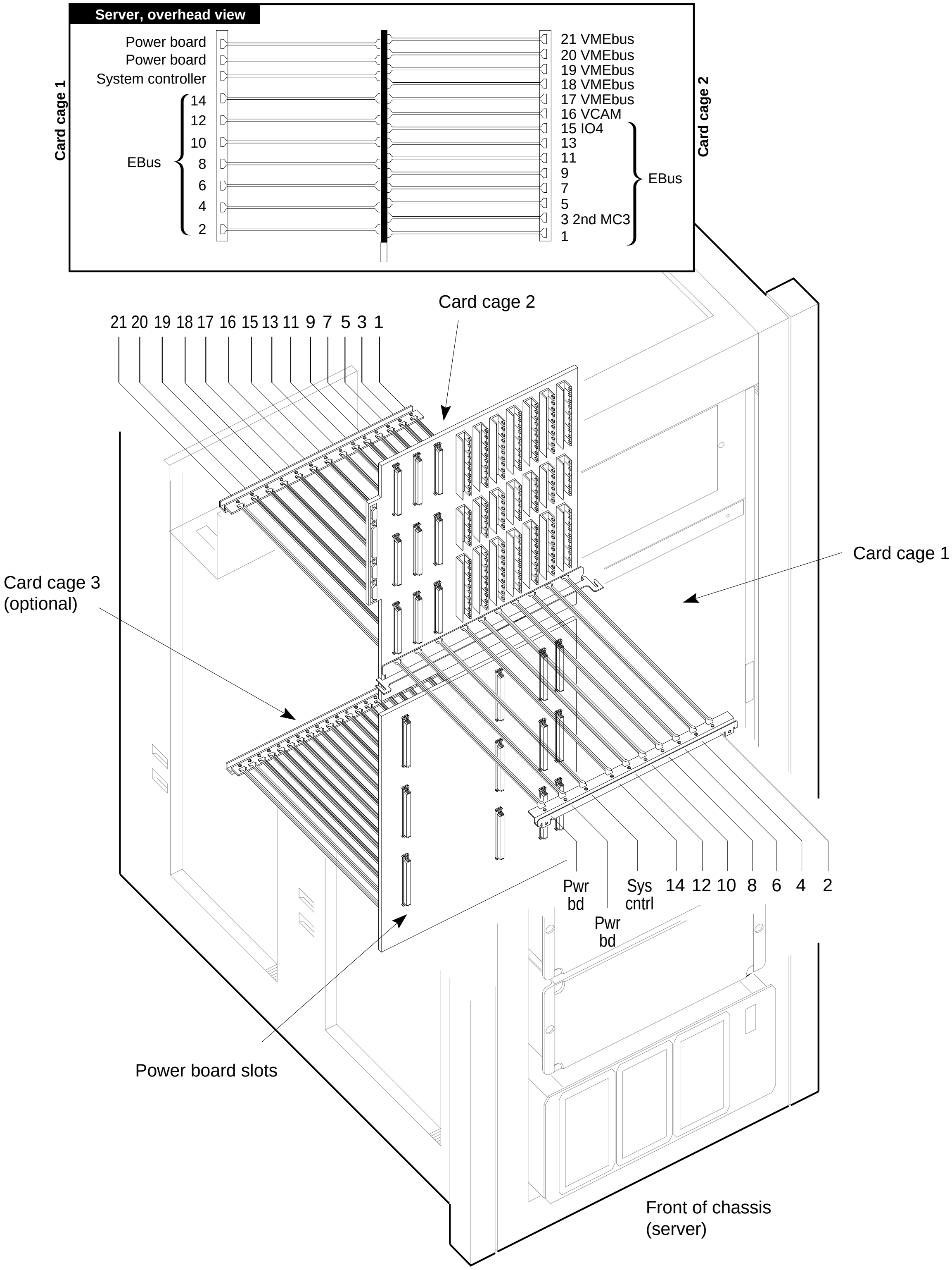


Figure 2-5 Challenge XL Card Cages and Slot Locations

2.4 Installation Procedure for Onyx Systems

This section describes the steps for installing FDDIXPress into an Onyx deskside or Onyx rackmount system. A maximum of three FDDIXPress boards can be installed into an Onyx deskside system; a maximum of four FDDIXPress boards can be installed into an Onyx rackmount system.

2.4.1 Prepare for Installation

1. Verify that the system's operating system version (IRIX or *eoe1*) matches the version of FDDIXPress that you are going to install. Software compatibility information is located in the *FDDIXPress Release Notes*. If necessary, upgrade the operating system.
2. Once the system is ready to install FDDIXPress, perform a system backup and verify the saved files.

2.4.2 Install and Configure Software

1. Use this command to verify that the FDDIXPress software has been installed:

   ```
   % /usr/sbin/versions FDDIXPress
   I   FDDIXPress   date   FDDIXPress version Option
   ```

   If the software is installed and the version is correct, proceed to the next step.

   If the message `Nothing satisfies the selection criteria` is displayed or if the version is not correct, install the FDDIXPress software, using the IRIX installation method and the Inst commands **install FDDIXPress** and **go**.
2. Configure the FDDI network interface, as explained in the *FDDIXPress Release Notes* or in Chapter 2 of the *FDDIXPress Administration Guide*.

2.4.3 Configure the Board

1. If you are installing more than one FDDIXPress board, verify that each board's **JA11** jumper is set to a unique unit number. Refer to Figure 1-2 for details.
2. Attach the board's cables (one optical bypass switch cable and two fiber optic cables) to the board.

   Each of the two fiber optic cables has a pair of ST connectors (each marked with an arrow indicating the direction of its signal). The ST connectors must be attached as illustrated in Figure 1-1, making sure to match cable **A** to the board's port A receptacles and cable **B** to the board's port B receptacles.

   Caution: If the ST connectors are not connected properly, the FDDI connection will not work.

   Attach the optical bypass switch cable to the board, as illustrated in Figure 2-2.
3. Disconnect the MIC connectors (on the fiber optic cables) from their previous mounting plates (two plates). Then, attach both MICs to the Challenge mounting plate (only one). Be sure to match the MICs to the labels on the plate.

4. Attach the optical bypass switch cable to the new mounting plate.

2.4.4 Install the Hardware

1. Shut down the system according to the operating system instructions.
2. Turn off the power key and unplug the power cable.
3. Remove all cables from the I/O door.
4. Open the I/O door on the system.

   Caution: The components are extremely sensitive to ESD (electrostatic discharge). Use proper antistatic procedures while handling all components.

5. Select a VMEbus slot for the FDDIXPress board. It is recommended that you use the first available VMEbus slot. For an Onyx deskside system, refer to Table 2-9 and Figure 2-6 for VMEbus slot information. For an Onyx rackmount system, refer to Table 2-10 and Figure 2-7.
6. Verify that a power supply board has been installed for the VMEbus slot(s) you have selected. On an Onyx deskside system, VMEbus power supply boards are installed at the back of the system, on the other side of the VMEbus connectors. On an Onyx rackmount system, VMEbus power supply boards are installed in card cage 1.
7. Install the FDDIXPress board and extender board into the VMEbus slot. The side of the board with the majority of the components faces to your right, as illustrated in Figure 2-1.
8. If you decide not to use the first available VMEbus slot, follow the instructions in the system's installation instruction manual to jumper the empty slots.
9. Attach the mounting plate to the I/O panel door.
10. Close the I/O door on the system.
11. Finish the installation following the instructions in Section 2.5, "Completing Board Installation."

Table 2-9 Onyx Deskside Board Slot Allocations

Slot Number	Board
1	Not to be used for VMEbus boards
2	Not to be used for VMEbus boards
3	Not to be used for VMEbus boards
4	IO4 and VCAM (VMEbus Channel Adapter Module)
5	First VMEbus board
6	Second VMEbus board
7	Third VMEbus board
8	Not to be used for VMEbus boards
9	Not to be used for VMEbus boards
10	Not to be used for VMEbus boards
11	Not to be used for VMEbus boards
12	Not to be used for VMEbus boards
13	Not to be used for VMEbus boards

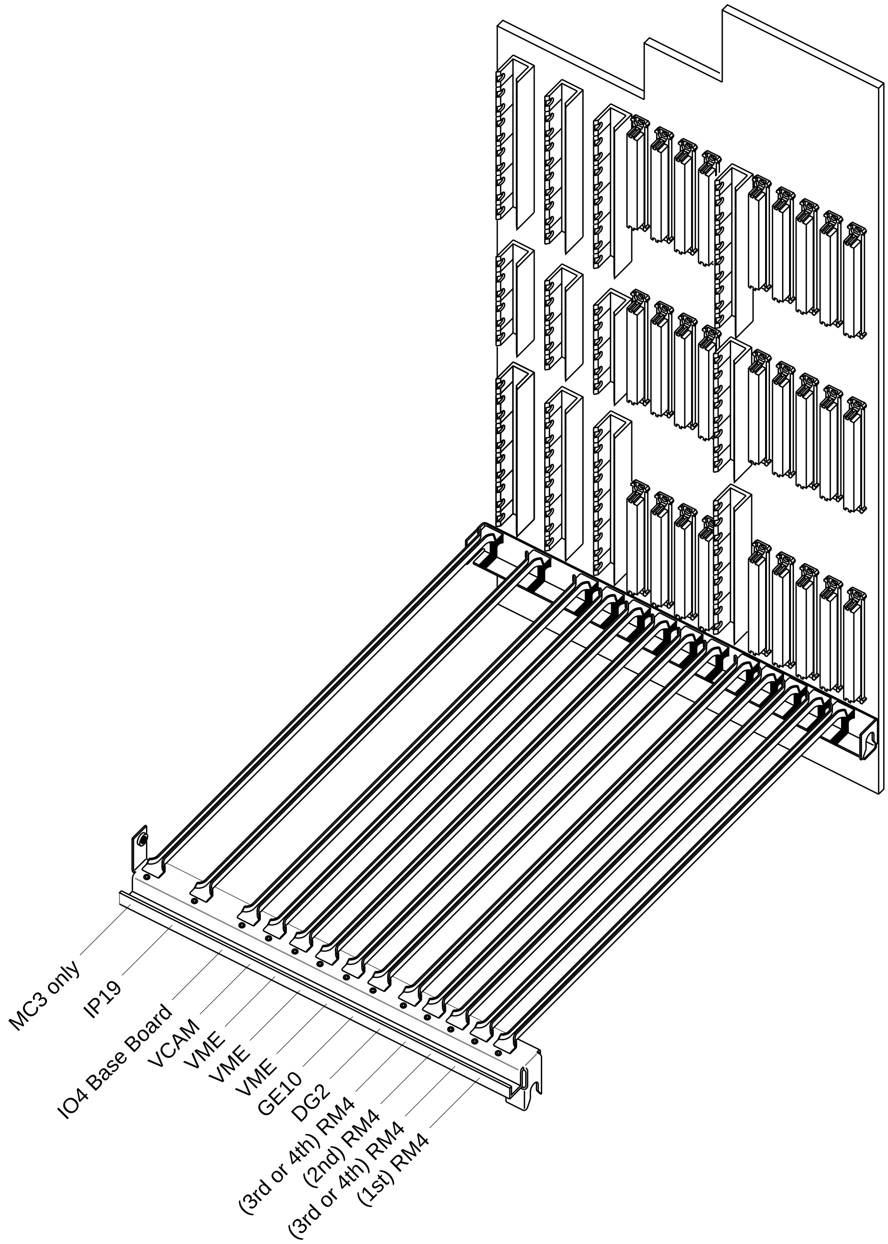


Figure 2-6 Onyx Deskside Slot Locations

Table 2-10 Onyx Rackmount Board Slot Allocations

Slot Number / Card Cage	Board
1 Card Cage 2	Not to be used for VMEbus boards
2 Card Cage 1	Not to be used for VMEbus boards

Table 2-10 Onyx Rackmount Board Slot Allocations

Slot Number / Card Cage	Board
3 Card Cage 2	Not to be used for VMEbus boards
4 Card Cage 1	Not to be used for VMEbus boards
5 Card Cage 2	Not to be used for VMEbus boards
6 Card Cage 1	Not to be used for VMEbus boards
7 Card Cage 2	Not to be used for VMEbus boards
8 Card Cage 1	Not to be used for VMEbus boards
9 Card Cage 2	Not to be used for VMEbus boards
10 Card Cage 1	Not to be used for VMEbus boards
11 Card Cage 2	Not to be used for VMEbus boards
12 Card Cage 2	IO4 and VCAM (VMEbus Channel Adapter Module)
13 Card Cage 2	First VMEbus option board
14 Card Cage 2	Second VMEbus option board
15 Card Cage 2	Third VMEbus option board
16 Card Cage 2	Not to be used for VMEbus boards
17 Card Cage 2	Not to be used for VMEbus boards
18 Card Cage 2	Not to be used for VMEbus boards
19 Card Cage 2	Not to be used for VMEbus boards
20 Card Cage 2	Not to be used for VMEbus boards
21 Card Cage 2	Not to be used for VMEbus boards

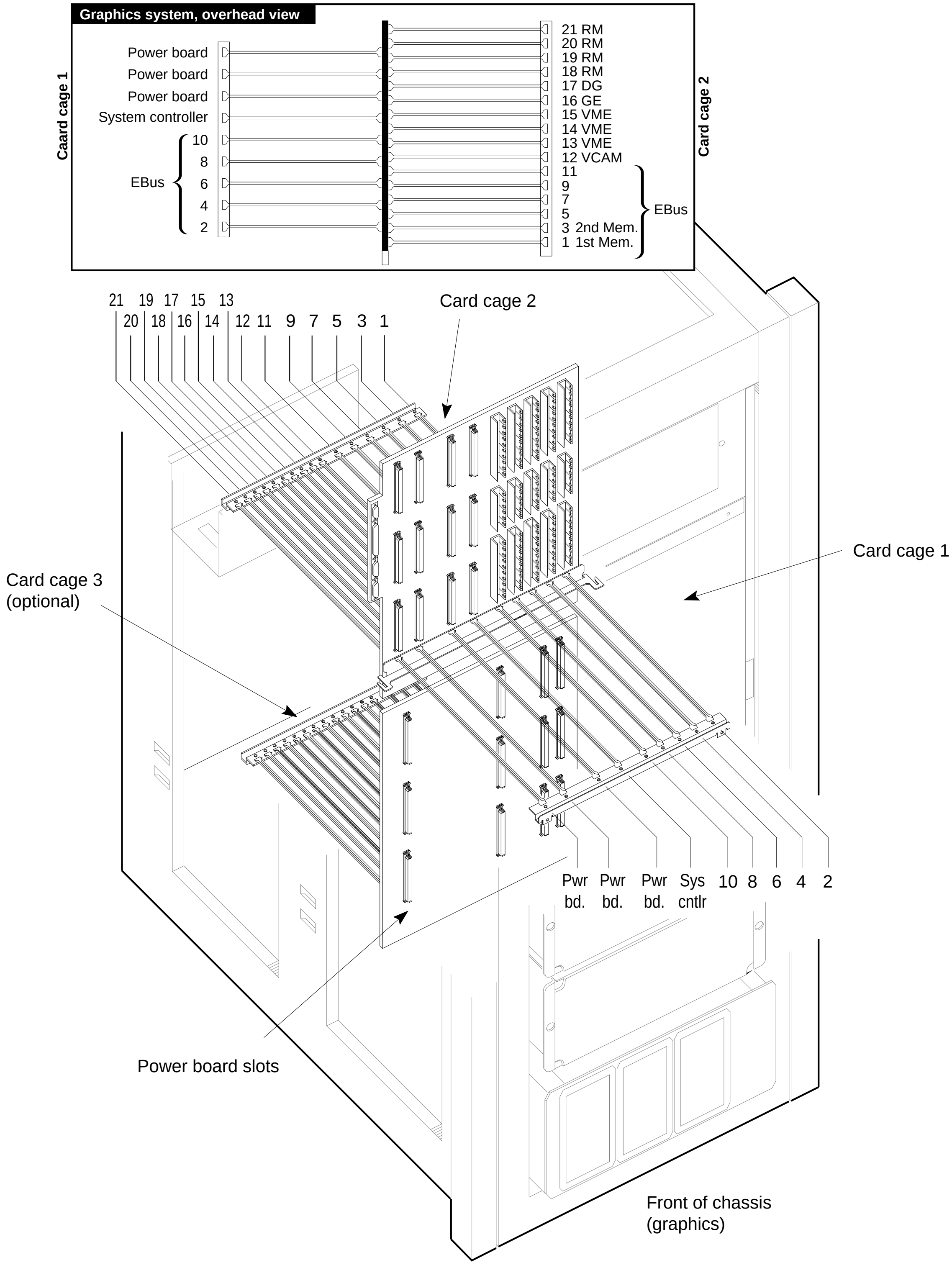


Figure 2-7 Onyx Rackmount Slot Locations

2.5 Completing Board Installation

Once you have installed the board(s), follow these steps. It is important to verify that each board is working properly before you connect the new FDDI station to the site's ring.

1. Ensure that the I/O door is closed.
2. Connect the main power cord.
3. Attach all previously removed cables to the I/O panel.
4. Turn on the main power switch.
5. If the Power On tests pass, access the System Maintenance Menu; type **`1`** to start the operating system.
6. When prompted with `Automatically rebuild the operating system?`, respond **yes**. This step builds the FDDIXPress driver (*ipg* driver) into the kernel.
7. When the system comes up again, access the System Maintenance Menu and again start the operating system. This second restart boots from (starts using) the newly built operating system.
8. Log on.
9. If you are using a graphical display monitor, open a window shell. For nongraphics systems, go to the next step.
10. At the prompt, type **`/bin/hinv`**. You should get a display similar to the following:

```
1 50 MHZ IP17 Processor
FPU: MIPS R4010 Floating Point Chip Revision: 0.0
CPU: MIPS R4000 Processor Chip Revision: 2.2
On-board serial ports: 4
Data cache size: 8 KBytes
Instruction cache size: 8 KBytes
Secondary unified instruction/data cache size: 1 MByte
Main memory size: 16 MBytes
I/O board, slot F: IO3B
Integral Ethernet: et0, IO3
FDDIXPress Controller; ipg0, Version 1
FDDIXPress Controller; ipg1, Version 1
IRIS TokenRing controller fv0: 16 Mbit
VGX Graphics option installed
Integral SCSI controller 1: Version WD33C93A, revision 9
Tape drive: unit 2 on SCSI controller 0: QIC 150
Disk drive: unit 1 on SCSI controller 0
Integral SCSI controller 0: Version WD33C93A, revision 9
```

Note: You must issue the */bin/hinv* command from the operating system, not the PROM monitor.

11. Verify that the `FDDIXPress Controller` line is displayed.
12. Connect the MICs on the I/O panel to the site's matching MICs (A-to-A and B-to-B when connecting directly to the dual ring or B-to-S when connecting to one M port on a concentrator or A-to-S and B-to-S when connecting to two M ports).
13. Verify that the FDDI network connection is functional by following the instructions in Chapter 2 of the *FDDIXPress Administration Guide*.

2.6 Connecting the Optional Bypass Switch

The optional optical bypass switch (OBS) maintains the integrity of the ring when the attached system becomes dysfunctional or disabled. To install the OBS, see the installation instructions that accompanied the OBS.

Chapter 3

Cabling

This chapter discusses FDDI cabling.

3.1 Site Cabling

It is recommended that the cabling for buildings be performed by a Silicon Graphics approved vendor. Adapter cables and other required accessories can also be obtained from approved vendors. For additional information on approved vendors, contact your Silicon Graphics sales office.

3.2 Media Interface Connectors

FDDI media interface connectors (MICs) each contain two fiber optic lines (an input and output). MICs are constructed so that invalid connections are very difficult to make. The connector ridge or cavity (as viewed from the front of the MIC) designates the connector type and mates only with the MIC that results in a valid connection.

3.3 ST Connectors

FDDI ST connectors each contain a single fiber optic line. Unlike MICs, ST connectors are not constructed in a manner that prevents invalid connections, you must be careful to determine that the signal direction through each connection is correct and to match the connections for primary and secondary rings.

3.4 Calculating Signal Decibel Loss

Insertion loss, interconnection loss, and link loss are all factors that must be calculated to determine signal decibel loss within the network. Use the following tables to calculate this factor.

Note: The maximum allowable total signal loss is 11 dB between stations.

Table 3-1 shows typical power losses from the possible sources. These values may vary, so it is highly recommended that actual measurements be taken.

Table 3-1 shows how to make signal loss calculations. Remember, this example shows only possible loss values. To ensure accuracy, you must make actual measurements.

The margin factor in Table 3-2 is derived by subtracting the total calculated signal loss (9.5) from the maximum amount allowed (11 dB). A remainder of 1.5 dB indicates that the signal loss is safely with the limit. Table 3-3 provides data for calculating link losses.

Table 3-1 Typical Power Losses

Factor	Power Loss per Unit	Example Unit (km)	Example Loss
Fiber Loss	2.5 dB/km	1	2.5 dB
Splice Loss	0.2 to 0.5 dB each	2	1.0 dB
Connector Loss	0.3 to 0.7 dB each	4	2.8 dB
Bypass Control Switch Loss	2.5 to 3.2 dB each	1	3.2 dB
Total Loss			9.5 dB
Margin Factor			1.5 dB

Table 3-2 Margin Factor

Factor	Margin per Unit	Example Unit (km)	Example Margin
Fiber Loss	2.5 dB/km	1	2.5 dB
Splice Loss	0.2 to 0.5 dB each	2	1.0 dB
Connector Loss	0.3 to 0.7 dB each	4	2.8 dB
Bypass Control Switch Loss	2.5 to 3.2 dB each	1	3.2 dB
Total Loss			9.5 dB
Margin Factor			1.5 dB

Table 3-3 Link Loss Calculation

Factor	Amount
Fiber Loss	2.5 dB/km
Splice Loss	0.2 to 0.5 dB each
Connector Loss	0.3 to 0.7 dB each

Table 3-3 Link Loss Calculation

Factor	Amount
Bypass Control Switch Loss	2.5 to 3.2 dB each

Chapter 4

Principles of Operation

4.1 Overview

The FDDIXPress network controller board is a RISC-based, high-performance node processor that connects the host to an FDDI network and processes the transmission and reception of data across the network.

4.1.1 Features

Features of the controller board include:

- AMD SUPERNET Chip Set
  The FDDIXPress Controller board uses a subset of this chip set.
- 1 MB Communications Buffer
  The Controller board has a one-megabyte communications buffer to help eliminate data overrun.
- On-Board RISC Processor
  AMD's Am29000 RISC microprocessor is capable of operating at 14 MIPS (millions of instructions / second).
- High-Performance VMEbus Interface
  The contoller board uses high-speed FIFO memory buffers and an asynchronous state machine that monitors VMEbus signalling.

4.2 Hardware Description

Refer to Figure 4-1 during the following discussion.

4.2.1 Optical Interface and Encoder/Decoder

The optical interface is provided by the Am7984A ENDEC and the Am7985A EDS . The optic interface chips connect directly to the optic transmitter and receiver through differential ECL drivers and receivers in the ENDEC and EDS parts.

An I/O port with high current sink capability is provided for controlling an external optical bypass switch. The switch bypasses the board in the case of a power failure. It can also take the node off the ring for diagnostic purposes, without causing the ring to wrap.

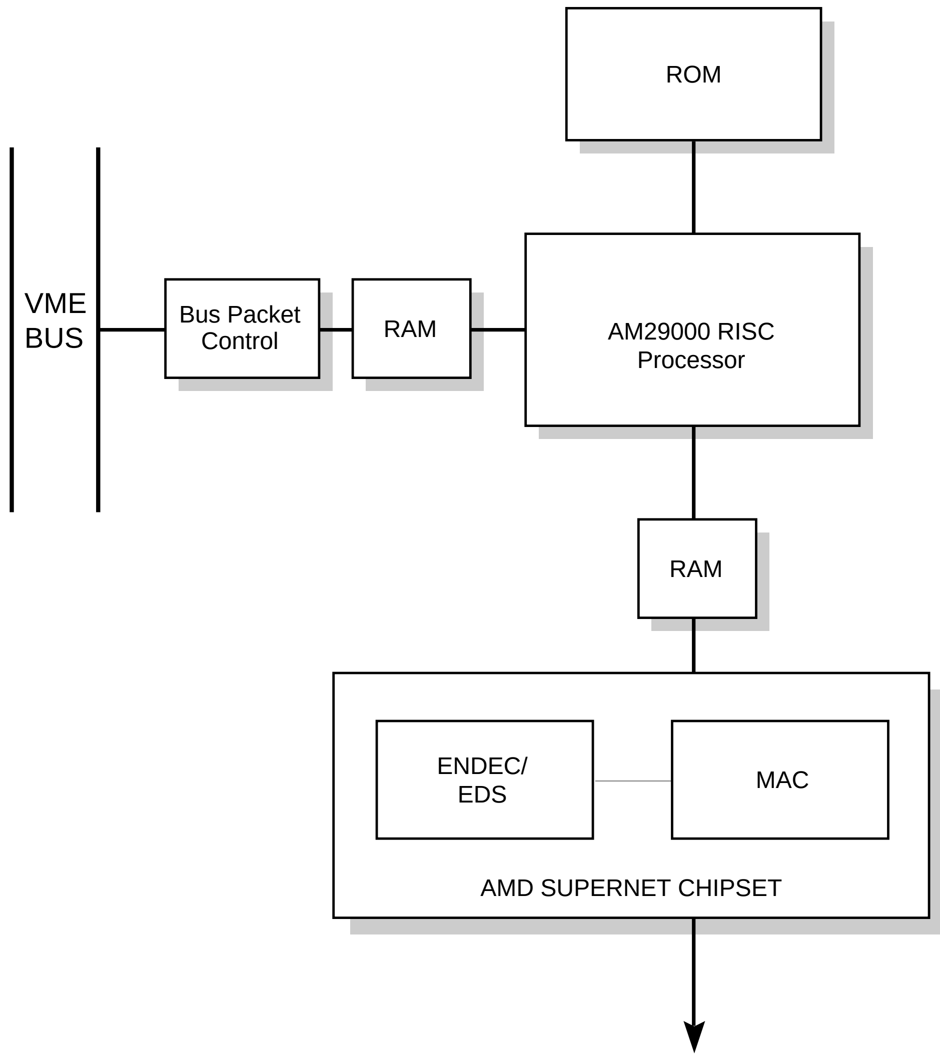


Figure 4-1 FDDIXPress Controller Board Block Diagram

The ENDEC component implements the 4B/5B encoding/decoding as specified by the ANSI X3T9.5 FDDI standard. It supports a 100 Mbps data rate with a 125 Mbaud serial output, and incorporates an internal elastic store buffer to compensate for clock mismatch. It also regenerates the incoming data string for transmission to the next host on the ring and inserts idle symbols into the stream if error is detected. The Am7984/Am7985A supports selectable loopback and repeat modes.

The EDS contains the clock generator, the Phase Lock Loop, and the data retimer. The clock inputs are selectable from a crystal, a TTL clock source, or a differential BCLK (byte clock). The data retimer removes the jitter component from the recovered data and aligns it with the negative of the recovered clock. The encoded output is selectable as NRZ or NRZI.

An I/O port with high current sink capability (up to 400 ma) is provided for controlling an external optical bypass switch. The port is available to the user via a right 2X2 Berg connector near the VMEbus front panel.

4.2.2 Media Access Control Chip

The AMD media access control (MAC) chip is the Am79C83 FORMAC. The main function of the MAC controller is to provide access to the FDDI network. The MAC is responsible for receiving incoming frames as well as capturing the token for transmitting frames.

In the receive mode, the MAC does the following:

- strips away the physical layer headers before sending the frame to the receive FIFO
- compares the destination address, and notifies the Rx State machine if the destination address does not match
- performs a CRC on the frame
- generates status bits that identify receiver line conditions and frame status, and strips away the end-of-frame characters
- compares the source address field

If the FORMAC identifies the source address as its own, it strips the remaining characters from the ring and replaces them with an idle pattern. Provision is made for using content addressable memory for decoding group addresses. The FORMAC supplies two 8-bit data buses parity (rx and tx) for buffer memory storage; the rx bus is tri-stateable.

In the transmit mode, the FORMAC captures the token, generates the physical layer headers, supplies the source address, generates the frame check sequence (CRC), and provides the ending delimiter and frame status.

The FORMAC also supplies the control for performing external source and destination address detection circuitry. This is necessary in bridging applications where the destination address is not present on the original FDDI ring. Signals are also present for generating ring statistics (such as error counts, line conditions, and so on).

The FORMAC contains the timers required to regulate the operation of the ring. These timers determine the length of time the host can hold the token (THT), the average time it takes the token to circulate around the ring (TRT), and a valid-transmission timer (TVX) to recover from transient ring error situations.

4.2.3 Buffer Memory

The buffer memory is an interim storage area for received frames and is used to buffer packets for transmission. It is composed of four sections: the DMA controller gate array, the elastic store buffer, the dynamic RAM controller and page-mode state machine, and the video DRAM memory.

4.2.4 Video DRAM Memory

The buffer memory consists of 1 MB of video dynamic RAM. Access to the random side of the memory is available by the Am29K microprocessor, the DMA controller gate array, and the VMEbus. Access to the serial side is available to the BUSpacket state machine.

The buffer memory is used for FDDI transmit and receive frames, the front end I/I descriptor rings, the VMEbus descriptor rings, and VMEbus short I/O.

4.2.5 Arbitration

All of the on-board arbitration is done in the DMA Controller Gate Array.

Since all front end memory cycles and some processor memory cycles are page-mode, all other sources are locked out of memory once a page-mode cycle is started. A request from another source is acknowledged at the end of a cycle.

Refresh has priority over all memory requests except for a memory cycle already in progress. When a memory cycle is running and a refresh request is made, the refresh request is handled at the end of the current cycle.

4.2.6 Microprocessor

The microprocessor is the AMD Am29000 RISC processor running at 16 MHz. This is a high performance RISC processor with separate buses for data and instruction cycles. Most instructions execute in one clock cycle.

4.2.7 RAM

There are 256KB of static RAM organized as 32K x 32 which is used to store the downloaded ROM code. This is attached to the processor’s instruction data bus.

Since scratch pad RAM is in the DRAM buffer memory, the access time to the processor may be delayed if another source is currently using the RAM. The worst access time occurs when the front end is doing a page-mode burst to memory.

4.2.8 PROM and EPROM

Two types of PROMs are used on the board. One type consists of four 32 x 8 PROMs to boot load the processor. The other is a single 64K x 8 EPROM that contains the board operation programs and online and offline diagnostics. After the processor is booted the EPROM code is downloaded into the microprocessor’s instruction memory. The ROM size can be increased to 128K x 8.

4.2.9 NVRAM

A 256K x 1 non-volatile RAM module stores the 48-bit IEEE-assigned MAC address. The assigned address is globally unique to every FDDI board.

4.2.10 Address Bus

Two address buses exist on the board. The instruction bus is 20 bits wide and is used exclusively by the processor to access instruction memory.

The random bus is 24 bits wide and is used to access the buffer memory VRAMs, the DMA Controller Gate Array, the on-board control registers, the SMT counters, and the FDDI controller chips. This bus is also used by the DMA Controller Gate Array and for the VMEbus short I/O.

4.2.11 Data Bus

Four independent data buses exist on the FDDI board; three of them are 32 bits wide. One is the processor instruction data bus which interfaces to static RAM. The second is the processor data bus, which is the local data bus. The third is the random data bus that interfaces to the random side of the buffer memory video RAMs.

The fourth is the serial side of the buffer memory video RAM that interfaces to the VMEbus. This bus is 16 bits wide. VMEbus master data transfers can be 32 bits wide but the internal transfer is two 16 bit accesses through this bus.

4.2.12 BUSpacket Control

The BUSpacket circuitry is an asynchronous state machine that handles the transfer of data across the VMEbus. The BUSpacket state machine functions only when the FDDI board is a bus master. The BUSpacket state machine is enabled when it receives the VMEbus starting address and address modifiers. The state machine can do byte, word, or longword transfers across the VMEbus, but all block mode transfers are in longword mode. Word transfers are possible between buffer memory and the VMEbus. Unaligned byte transfers are not supported.