Everest Core-Board Revision History

Document Number 108-0141-001

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Document Number 108-0141-001

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Introduction

This book describes the revision history of the core-boards used in the Everest product line, explains the reasons for various changes made to the boards throughout their history, and describes the implications of those changes to the field.

Note: This book does not provide a detailed description of the general function of the boards, does not (for the most part) discuss interactions between various boards, and does not address software issues.

This document presents technical details as accurately as possible. It does not describe service policy.

In a number of places within this document boards with different part numbers are said to be “functionally equivalent.” What this means is that the two boards are either identical (often this is due to a Bill Of Materials (“BOM”) correction), or that the two boards are so similar as to be interchangeable without concern about a change in functionality (this is often the case when the brand of a component changes, but the new component transparently replaces the old one).

In some places there are boards with revisions so closely related that discussion of those boards has been combined into the same paragraph. In other cases, some boards are dissimilar enough that discussing them together would be confusing. In these cases discussion of the boards has been separated into different paragraphs. This separation necessitates some duplication, but the increased clarity seems worth it.

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Chapter 1

IP19 Processor Board Revision History

Each IP19 processor board uses between one and four MIPS 64-bit R4400 processors. There may be as many as nine IP19 processor boards in one rack system and as many as three in a deskside system. IP19 processor boards have been made with one, two and four processors per board, running at CPU speeds of 100Mhz, 150Mhz, and 200Mhz, and with both 3V and 5V CPUs. They have been available with either 1 Megabyte per processor or with 4 Megabytes per processor of secondary cache RAM.

1.1 IP19 Board History

The IP19 processor boards started out at 100Mhz (using a 50Mhz clock oscillator) with 1 MB of secondary cache per processor, and were available with two or four processors (030-0249-004 and 030-0250-004, respectively) in March, 1993.

The first revision to the IP19 boards (030-0249-005 and 030-0250-005) removed the heatsinks from the CC ASICs and verified that all ASICs were fully seated.

Revisions 030-0249-006 and 030-0250-006 contained a new version of the Boot PROM, which enabled the IP19 boards to work with the new revision of the MC3 memory board.

Revisions 030-0249-007 and 030-0250-007 incorporated modifications designed to improve hold-time between the R4400 and the CC chip.

Revisions 030-0249-008 and 030-0250-008 incorporated changes designed to prevent corruption of the R4400 Configuration EAROM (Electrically Alterable ROM) on power-up, and detect and repair it if it happens. They also included a UART code fix for large SCSI systems (it no longer prints “U”s), fixed the “decode” command, and fixed the “Don’t clear memory” switch.

IP19 processor boards running at 150Mhz (using a 75Mhz clock oscillator) with 1 MB of secondary cache per processor were released with both two and four processors (030-0374-004 and 030-0375-004, respectively) in August, 1993.

In order to support Power Fortran, the IP19 board’s CC chips were changed in revisions 030-0249-010, 030-0250-010, 030-0374-006, and 030-0375-006. The changes were entirely backwardly compatible.

Revisions 030-0249-011, 030-0250-011, 030-0374-007A, and 030-0375-007A incorporated changes designed to eliminate corruption of the R4400 Configuration EAROM during power-down, and to reduce clock jitter.

A single-processor IP19, running at 150Mhz (using a 75Mhz clock oscillator) with 1 MB of secondary cache, was released as 030-0525-002 in December, 1993.

A single-processor IP19, running at 100Mhz (using a 50Mhz clock oscillator) with 1 MB of secondary cache, was released as 030-0642-001 in July, 1994. This board was primarily intended for use in the CHALLENGE DM system.

At the same time as the release of the 030-0642-001, instructions to update other IP19 boards to allow their use in CHALLENGE DM systems were released.

A new FAB (034-0345-002), which could be used to produce both 3V* and 5V IP19 boards, was used for 150Mhz IP19 boards starting with revisions 030-0374-008, 030-0375-008, and 030-0525-002. The BOMs were also changed to allow the use of the new FAB for the production of 100Mhz IP19 processor boards (030-0249-012, 030-0250-012, and 030-0642-001). Records indicate, however, that no 100Mhz IP19 boards were ever built on the newer FAB.

IP19 boards based on the new FAB (034-0345-002) caused boot failure when used in systems which also contained IP19 boards based on the old FAB (034-0250-003). This problem was corrected in revisions 030-0249-013, 030-0250-013, 030-0642-002, 030-0374-009, 030-0375-009, and 030-0525-004.

IP19 processor boards running at 200Mhz (using a 100Mhz clock oscillator) with 4 MB of secondary cache per processor were released with both two and four processors (030-0652-004 and 030-0653-004, respectively) in October, 1994.

A single-processor IP19, running at 200Mhz (using a 100Mhz clock oscillator) with 1 MB of secondary cache (unlike the other 200Mhz IP19 boards, which have 4 MB), was released in February, 1995 (030-0720-001A). This board was primarily intended for use in the Reality Station system.

1.2 IP19 Indications For Use

A problem in which the IP19 R4400 Configuration EAROMs were being overwritten at power-up was fixed in the IP19 boards in Group 5, Table 1-1Figure 1-1.

The first IP19 processor boards to support Power Fortran were those found in Group 6, Table 1-1Figure 1-1.

A problem in which the IP19 R4400 Configuration EAROMs were being overwritten at power-down was fixed in the IP19 boards in Group 7, Table 1-1Figure 1-1.

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* Although these are commonly called “3V” boards, the term is a bit misleading. On most “3V” IP19 boards the CPU is actually running at 3.45 volts.

Certain revisions of the IP19 processor board based on the newer FAB (034-0345-002) have a boot problem when used in systems which also contain IP19 boards based on the older FAB (034-0250-003). This problem is only found in the IP19 boards in Group 9, Table 1-1Figure 1-1, and is not found in all of those boards. In later revisions the problem is corrected, and the later boards may be freely used in systems with IP19 boards based on the older FAB.

The CHALLENGE DM requires an IP19 with a CC-shared PAL version 070-1116-002 or later. This PAL is found on the IP19 boards in Group 9, Table 1-1Figure 1-1, and later, and on all of the 200Mhz IP19 boards.

The Reality Station requires the use of a single-CPU IP19 board. This is typically the 200Mhz 030-0720-001, but it will also work with any single-CPU IP19 from Group 9, Table 1-1Figure 1-1 or later.

It is likely that an upcoming version of the IRIX operating system will not run on IP19 processor boards with 100Mhz R4400 CPUs dated 9336 or earlier. When an IP19 is installed in a system the easiest way to tell the status of the CPU is to run an 'hinv.' R4400 revisions 5.0 or later will work with the new version of IRIX. R4400 revisions 4.0 or earlier will not.

Note: The revision numbers printed on some of the chips do not directly correspond to the revision numbers reported by hinv. Use either the revision reported by hinv, or the date printed on the chips.

Table 1-1Figure 1-1 and Table 1-2Figure 1-2 provide a quick-reference for the various changes made to the IP19.

Table 1-1 IP19 Board Quick-Reference (100 Mhz and 150 Mhz boards)

Group	100Mhz One CPU	100Mhz Two CPUs	100Mhz Four CPUs	150Mhz One CPU	150Mhz Two CPUs	150Mhz Four CPUs	Notes
1		030-0249-004	030-0250-004				
2		030-0249-005	030-0250-005				
3		030-0249-006	030-0250-006				Boot PROM
4		030-0249-007	030-0250-007				
5		030-0249-008	030-0250-008		030-0374-004	030-0375-004	
		030-0249-009	030-0250-009		030-0374-005	030-0375-005	
6		030-0249-010	030-0250-010		030-0374-006	030-0375-006	
7		030-0249-011	030-0250-011	030-0525-002	030-0374-007	030-0375-007	
9	030-0642-001	030-0249-012	030-0250-012	030-0525-003	030-0374-008	030-0375-008	Chal. DM min.
10	030-0642-002	030-0249-013	030-0250-013	030-0525-004	030-0374-009	030-0375-009	

Table 1-2 IP19 Board Quick-Reference (200 Mhz boards)

Group	200Mhz One CPU	200Mhz Two CPUs	200Mhz Four CPUs	Notes
1		030-0652-001	030-0653-001	
2	030-0720-001	030-0652-002	030-0653-002	

Group	100Mhz One CPU	100Mhz Two CPUs	100Mhz Four CPUs	150Mhz One CPU	150Mhz Two CPUs	150Mhz Four CPUs	Notes
1		030-0249-004	030-0250-004				
2		030-0249-005	030-0250-005				
3		030-0249-006	030-0250-006				Boot PROM
4		030-0249-007	030-0250-007				
5		030-0249-008	030-0250-008		030-0374-004	030-0375-004	
		030-0249-009	030-0250-009		030-0374-005	030-0375-005	
6		030-0249-010	030-0250-010		030-0374-006	030-0375-006	
7		030-0249-011	030-0250-011	030-0525-002	030-0374-007	030-0375-007	
9	030-0642-001	030-0249-012	030-0250-012	030-0525-003	030-0374-008	030-0375-008	Chal. DM min.
10	030-0642-002	030-0249-013	030-0250-013	030-0525-004	030-0374-009	030-0375-009	

Figure 1-1 IP19 Board Quick-Reference (100 Mhz boards)

Group	200Mhz One CPU	200Mhz Two CPUs	200Mhz Four CPUs	Notes
1		030-0652-001	030-0653-001	
2	030-0720-001	030-0652-002	030-0653-002	

Figure 1-2 IP19 Board Quick-Reference (200 Mhz boards)

1.3 IP19 Board Revisions

030-0249-004 and 030-0250-004: These were the first shipping versions of the IP19 processor board. The 030-0249-xxx boards have two processors, the 030-0250-xxx boards have four processors.

030-0249-005 and 030-0250-005: This revision verified that all ASICs were fully seated, added a wire at the CC chip's PLL-GND, and removed heatsinks from CC ASICs to improve yield.

030-0249-006 and 030-0250-006: This revision replaced IP19 Boot PROM version 10 (070-1122-010) with Boot PROM version 11 (070-1122-011). This allows the IP19 to work with an MC3 board which contains MA ASIC version 3, supporting full population of the

MC3's thirty-two SIMM banks (instead of only sixteen, as previously supported). The new PROM also includes improved POD "mem" test, and improved fault location in the "niblet" command.

030-0249-007A and 030-0250-007A: This revision incorporated board rework (adding a wire and removing a capacitor at each CPU) designed to improve the hold-time between the R4400 and the CC chip.

030-0249-007B and 030-0250-007B: This revision incorporated a socket change for future use. These IP19 boards are functionally equivalent to 030-0249-007A and 030-0250-007A, respectively.

030-0249-008 and 030-0250-008: This revision incorporated board rework to change the Write Enable on the R4400 Configuration EAROM from 3V to 5V to prevent inadvertent write at power-up. It also incorporated a new IP19 Boot PROM, replacing version 11 (070-1122-011) with version 13 (070-1122-013), and a new R4400 Configuration EAROM, replacing version 2 (070-1121-002) with version 3 (070-1121-003). The new Boot PROM included a UART code fix for large SCSI systems (it no longer prints "U"s), added code to detect and repair R4400 Configuration EAROM corruption where possible, fixed the "decode" command, and fixed the "Don't clear memory" switch. The new R4400 Configuration EAROM included a checksum to detect corruption.

030-0249-009 and 030-0250-009: This revision represented a documentation change only. These IP19 boards are functionally equivalent to 030-0249-008A and 030-0250-008A, respectively.

030-0249-010 and 030-0250-010: This revision replaced the Coherency Controller (CC) chips in order to support Power Fortran. The new chips (and thus the new boards) are entirely backwardly compatible.

030-0249-011A and 030-0250-011A: This revision incorporated a board rework which added an additional socket between the R4400 Configuration EAROM and its existing socket. The intermediate socket included a resistor pulling up the (lifted) write-enable pin. The rework also replaced some inductors with resistors in the PLL power circuitry. The write-enable change should prevent the R4400 Configuration EAROM from being overwritten (primarily a problem during power-down), and the PLL modifications should reduce clock jitter.

030-0250-011B: This revision simply represents a BOM correction. This IP19 board is functionally equivalent to 030-0250-011A.

030-0249-011B and 030-0250-011C: This revision removed the A and CC chip sockets for improved reliability. These IP19 boards are functionally equivalent to 030-0249-011A and 030-0250-011B, respectively.

030-0249-012A, 030-0250-012A, and 030-0642-001A: This revision incorporated a change in the BOMs allowing the production of 100Mhz IP19 boards (with one, two or four CPUs) using the newer FAB (034-0345-002). Records indicate, however, that no 100Mhz IP19 boards were built on the newer FAB. The revision also replaced version 1 of the CC-shared PAL (070-1116-001) with version 2 (070-1116-002). The new PAL makes these IP19 boards compatible with the CHALLENGE DM systems. Note that 030-0642-001A was the first

shipping version of the single-CPU 100Mhz IP19 board, and was primarily intended for use in the single-CPU configuration of the CHALLENGE DM.

030-0249-012B, 030-0250-012B, and 030-0642-001B: This revision applied only to IP19 boards built on the newer FAB (034-0345-002). It replaced a clock-driver chip (74FCT3244, SGI part # 9800715) with a different version (74LVT244, SGI part # 9001159), and corrected a number of minor BOM errors. The new clock-driver chip was simply intended to fix an LED failure problem, primarily found on CPU 2, which caused it to display incorrect values, or to remain blank. However, it turned out to be a more important change than anticipated (see next revision).

030-0249-013A, 030-0250-013A, and 030-0642-002: This revision does nothing other than change the part number. The previous revision, which replaced the clock-driver chip, was thought to be a minor change. However, it turned out to also fix a more serious problem at the same time. IP19 boards based on the new FAB (034-0345-002) with the 74FCT3244 chip have a latchup mode that can cause boot failure when used in a system that also contains IP19 boards based on the older FAB (034-0250-003). The replacement part, 74LVT244, is Bi-CMOS, and does not have the latchup problem. It was decided that this difference deserved a full number change, rather than simply a new letter.

030-0249-013B and 030-0250-013B: This revision simply represented a BOM restructuring. The 300-levels of these BOMs were eliminated. These IP19 boards are functionally equivalent to 030-0249-013A and 030-0250-013A, respectively.

030-0374-004 and 030-0375-004: These were the first shipping versions of the 150Mhz IP19 processor boards. The 030-0374-xxx IP19 boards have two processors, the 030-0375-xxx IP19 boards have four processors. Their functional level corresponds with that of 030-0249-008.

030-0374-005 and 030-0375-005: This revision represented a documentation change only. These IP19 boards are functionally equivalent to 030-0374-004 and 030-0375-004, respectively.

030-0374-006 and 030-0375-006: This revision replaced the Coherency Controller (CC) chips in order to support Power Fortran. The new chips are entirely backwardly compatible.

030-0374-007A, 030-0375-007A, and 030-0525-002A: This revision incorporated a board rework which added an additional socket between the R4400 Configuration EAROM and its existing socket. The intermediate socket included a resistor pulling up the (lifted) write-enable pin. The rework also replaced some inductors with resistors in the PLL power circuitry. The write-enable change should prevent the R4400 Configuration EAROM from being overwritten (primarily a problem during power-down), and the PLL modifications should reduce clock jitter. Note that 030-0525-002 is the first shipping version of the single-CPU 150Mhz IP19 board.

030-0375-007B: This revision simply represents a BOM correction. This IP19 board is functionally equivalent to 030-0375-007A.

030-0374-007B, 030-0375-007C, and 030-0525-002B: This revision removed the A and CC chip sockets for improved reliability. These IP19 boards are functionally equivalent to 030-0374-007A, 030-0375-007B, and 030-0525-002A, respectively.

030-0374-008A, 030-0375-008A, and 030-0525-003A: This revision began using a new FAB (034-0345-002) for the 150Mhz IP19 boards, and began the use of 3V CPUs on the IP19. It obsoleted a number of components no longer needed on the new FAB, and it replaced a number of 5V components with their 3V equivalents. This revision also replaced version 1 of the CC-shared PAL (070-1116-001) with version 2 (070-1116-002). The new PAL makes these IP19 boards compatible with the CHALLENGE DM systems.

030-0374-008B, 030-0375-008B, and 030-0525-003B: This revision was simply represents a BOM change. These IP19 boards are functionally equivalent to 030-0374-008A, 030-0375-008A, and 030-0525-003A, respectively.

030-0374-008C, 030-0375-008C, and 030-0525-003C: This revision applied only to IP19 boards built on the newer FAB (034-0345-002). It replaced a clock-driver chip (74FCT3244, SGI part # 9800715) with a different version (74LVT244, SGI part # 9001159), and corrected a number of minor BOM errors. The new clock-driver chip was simply intended to fix an LED failure problem, primarily found on CPU 2, which caused it to display incorrect values, or to remain blank. However, it turned out to be a more important change than anticipated (see next revision).

030-0374-009A, 030-0375-009A, and 030-0525-004A: This revision does nothing other than change the part number. The previous revision, which replaced the clock-driver chip, was thought to be a minor change. However, it turned out to also fix a more serious problem at the same time. IP19 boards based on the new FAB (034-0345-002) with the 74FCT3244 chip have a latchup mode that can cause boot failure when used in a system that also contains IP19 boards based on the older FAB (034-0250-003). The replacement part, 74LVT244, is Bi-CMOS, and does not have the latchup problem. It was decided that this difference deserved a full number change, rather than simply a new letter. Thus this revision.

030-0375-009B: Information on this revision will be included in the final draft of this document.

030-0374-009B and 030-0375-009C: This revision simply represented a BOM restructuring. The 300-levels of these BOMs were eliminated. These IP19 boards are functionally equivalent to 030-0374-009A and 030-0375-009B, respectively.

030-0525-00x: These single-processor IP19 boards are included in this listing along with the 030-0374-xxx and 030-0375-xxx IP19 boards (above).

030-0642-00x: These single-processor IP19 boards are included in this listing along with the 030-0249-xxx and 030-0250-xxx IP19 boards (above).

030-0652-001A and 030-0653-001A: These were the first shipping versions of the 200Mhz IP19 processor boards, and contain 4 MB secondary cache per processor. The 030-0652-xxx IP19 boards have two processors, the 030-0653-xxx boards have four processors.

030-0652-001B and 030-0653-001B: This revision was simply a BOM restructuring. The 300-levels of these BOMs were eliminated. These IP19 boards are functionally equivalent to 030-0652-001A and 030-0653-001A, respectively.

030-0720-001A: This was the first shipping version of the single-CPU 200Mhz IP19 board. Unlike the 030-0652-00x and the 030-0653-00x, this IP19 board only has 1 MB of secondary cache. This IP19 board was primarily intended for use in the Reality Station.

Chapter 2

IP21 Processor Board Revision History

The IP21 processor board uses one or two 64-bit MIPS R8000 processors. There may be as many as nine IP21 processor boards in one rack system and as many as three in a deskside system. The IP21 provides significantly greater performance than the IP19 processor board.

The R8000 processor (sometimes called the TFP processor) is actually a two-chip set: an Instruction Unit (IU) and a Floating-Point Unit (FPU). These two chips have sometimes been referred to as the R8000 and the R8010, respectively.

The IP21 is available in single- or dual-processor versions, both running at a CPU speed of 75 Mhz. All IP21 boards use 3 volt* technology, and all have 4 Megabytes of secondary cache RAM for each CPU. The IP21 processor board's cache SIMMs are soldered in place, unlike those on the IP19 processor board (which are socketed).

2.1 IP21 Board History

The 030-0636-xxx boards are the 75 Mhz single-CPU versions of the IP21, and the 030-0625-xxx boards are the 75 Mhz dual-CPU versions of the IP21. Both are based on the 034-0625-003 FAB.

Approximately twenty 75 Mhz dual-CPU boards were shipped to beta customers and SGI field offices before the IP21 MR'ed. These boards, P/N 030-0625-002, 030-0625-003, and 030-0625-105, were beta-release boards. If one of these boards is found in the field with a problem, contact SSD engineering. These boards should only be returned via the beta upgrade program.

Both the single- and dual-CPU versions of the 75 Mhz IP21 boards were officially released in August, 1994

Due to a problem with many of the Instruction Units (IUs), a heater and thermostat combination was added in revisions 030-0625-107 and 030-0636-005 of the IP21 board. The IU heater/thermostat combination was retained until revisions 030-0625-112 and 030-0636-009.

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* Although these are commonly called "3V" boards, the term is a bit misleading. On the IP21 boards the CPU is actually running at 3.45 volts.

A write-gather problem in revision C of the Cache Controller (BBCC) chip (099-0062-003) prompted a new revision of the dual processor IP21 (030-0625-108) with a new version of the BBCC chip (revision D, 099-0062-004). Note that the write-gather problem does not affect server systems, and thus revision 030-0625-108 was only shipped in graphics systems.

To improve manufacturing yields, the thermostat temperature for the IU heater was increased in revisions 030-0625-109 and 030-0636-007 of the IP21 boards. At the same time, 030-0625-110 was released for use in graphics systems. This board is the same as 030-0625-109 with the addition of revision D BBCC chips.

In order to eliminate a boot problem, the boot PROM was updated in revisions 030-0625-111 and 030-0636-008 of the IP21 boards.

A design change to the R8000 eliminated the need for the IU heater and its associated thermostat in revisions 030-0625-112 and 030-0636-009 of the IP21 boards.

Single- and dual-CPU 90 Mhz IP21 boards were released in May, 1995. The 030-0703-xxx boards are the 90 Mhz single-CPU versions of the IP21, the 030-702-xxx boards are the 90 Mhz dual-CPU server versions of the IP21, and the 030-0858-xxx boards are the 90 Mhz dual-CPU graphics versions of the IP21. All three are based on the 034-0702-002 FAB.

The initial release of the 90 Mhz IP21 included three versions of the board. The single-CPU version, 030-0703-002, has revision D of the BBCC chip (099-0062-004) and is therefore usable in graphics and server systems. One of the dual-CPU versions, 030-0702-002, uses revision C of the BBCC (099-0062-003), and is therefore only suitable for use in server systems. The other dual-CPU version, 030-0858-001, uses revision D of the BBCC, and is therefore suitable for use in both graphics and server systems.

2.2 IP21 Indications For Use

A number of IP21 processor boards used BBCC (BlackBird Cache Controller) chips that had a write-gather problem in multi-processor graphics systems. All multi-processor graphics systems should use IP21 boards with the newer version of the BBCC. The IP21 boards with this problem are indicated by shaded entries in Table 2-1Figure 2-1.

Note: A single-processor IP21 board with a revision C BBCC chip may be used in a graphics system, but only if it is the only processor board in the system. This is a typical configuration for deskside Power Onyx systems, which only have room for one processor board anyway. It is only if the single-processor IP21 board is replaced with a dual-processor IP21 board that the BBCC-chip revision becomes an issue.

A new boot PROM, used on 030-0625-111 and 030-0636-008 (and subsequent) IP21 boards eliminated a problem in which the system hung during CC write-gather tests at boot-up.

Table 2-1Figure 2-1 provides a quick-reference for the various changes made to the IP21.

Figure 2-1 IP21 Board Quick-Reference

Indications	75Mhz Single-CPU	75Mhz Dual-CPU	90Mhz Single-CPU	90Mhz Dual-CPU	Notes
Boot PROM problems		030-0626-002			Beta revision
		030-0626-003			Beta revision
		030-0626-105			Beta revision
		030-0625-106			First MR
	030-0636-005	030-0625-107			Added IU heater
		030-0625-108			New BBCC chip
	030-0636-007	030-0625-109			New therm., old
		030-0625-110			New therm., new
Boot PROM fixed	030-0636-008	030-0625-111			New boot PROM
	030-0636-009	030-0625-112			New IU, no IU he
				030-0702-002	Old BBCC chip
			030-0703-002	030-0858-001	New BBCC chip

Table 2-1 IP21 Board Quick-Reference

Indications	75Mhz Single-CPU	75Mhz Dual-CPU	90Mhz Single-CPU	90Mhz Dual-CPU	Notes
Boot PROM problems		030-0626-002			Beta revision
		030-0626-003			Beta revision
		030-0626-105			Beta revision
		030-0625-106			First MR
	030-0636-005	030-0625-107			Added IU heater
		030-0625-108			New BBCC chip
	030-0636-007	030-0625-109			New therm., old BBCC
		030-0625-110			New therm., new BBCC
Boot PROM fixed	030-0636-008	030-0625-111			New boot PROM
	030-0636-009	030-0625-112			New IU, no IU heater
				030-0702-002	Old BBCC chip
			030-0703-002	030-0858-001	New BBCC chip
Don't use shaded boards in multi-processor graphics systems					

2.3 IP21 Board Revisions

030-0625-002: This was a beta revision. If found in the field with a problem, contact SSD engineering. These boards should only be returned via the beta upgrade program.

030-0625-003: This was a beta revision. If found in the field with a problem, contact SSD engineering. These boards should only be returned via the beta upgrade program.

030-0625-105: This was a beta revision. If found in the field with a problem, contact SSD engineering. These boards should only be returned via the beta upgrade program.

030-0625-106: This was the first revision of the IP21 board to officially ship, and it is based on the 034-0625-003 FAB. It used Instruction Units (IUs) which were not susceptible to the FastIU problem. These Instruction Units may be identified by their blue stripe. This revision is not suitable for use in graphics systems due to a BBCC-chip problem.

030-0625-107: This revision incorporated a thermostatic control unit and a chip-heater for the Instruction Unit. These measures were needed in order to eliminate the FastIU problem in those Instruction Units so affected. Affected Instruction Units are marked with a white or red stripe. If an Instruction Unit has a blue stripe, there is no need for the heater. This revision is functionally equivalent to 030-0625-109. It is not suitable for use in graphics systems due to a BBCC-chip problem.

030-0625-108: This revision incorporated a new version of the BBCC chip (P / N 099-0062-004). This new version eliminates a write-gather problem in multi-processor graphics systems. This is therefore the first dual-processor IP21 board suitable for use in either graphics or server system (note, however, that the following full revision, 030-0625-109, may not be used in a graphics system). This revision is functionally equivalent to 030-0625-110.

030-0625-109: This revision used a new version of the thermostat control board (P / N 030-0691-003) which incorporated a slight change in the Instruction Unit temperature. This should not affect the field. This revision is functionally equivalent to 030-0625-107. Due to a shortage of new BBCC chips, this revision contained the older version of the BBCC chips. It is therefore not suitable for use in graphics systems.

030-0625-110: This revision used a new version of the thermostat control board (P / N 030-0691-003) which incorporated a slight change in the Instruction Unit temperature. This should not affect the field. This revision is functionally equivalent to 030-0625-108. It used the newer BBCC chips, and is therefore suitable for use in graphics or server systems.

030-0625-111: This revision used a new version of the boot PROM. This eliminated a problem in which the system hung during CC write-gather tests at boot-up. This board is functionally equivalent to 030-0625-112. It used the newer BBCC chips, and is therefore suitable for use in either graphics or server systems.

030-0625-112: This revision used a new version of the Instruction Unit chip (P / N 098-0003-004) which eliminated the FastIU problem. It therefore did not need a thermostat control board or a chip heater. This board is functionally equivalent to 030-0625-111. It used the newer BBCC chips, and is therefore suitable for use in either graphics or server systems.

030-0636-005: This revision incorporated a thermostatic control unit and a chip-heater for the Instruction Unit. These measures were needed in order to eliminate the FastIU problem in those Instruction Units so affected. Affected Instruction Units are marked with a white or red stripe. If an Instruction Unit has a blue stripe, there is no need for the heater. This revision is functionally equivalent to 030-0636-007. This board had a BBCC-chip problem,

and therefore may be used in a graphics system only if it is the only processor board in the system.

030-0636-006: This number was used for a prototype board. None were shipped.

030-0636-007: This revision used a new version of the thermostat control board (P / N 030-0691-003) which incorporated a slight change in the Instruction Unit temperature. This should not affect the field. This revision is functionally equivalent to 030-0636-005. Due to a BBCC-chip problem, this board may be used in a graphics system only if it is the only processor board in the system.

030-0636-008: This revision used a new version of the boot PROM. This eliminated a problem in which the system hung during CC write-gather tests at boot-up. Due to a BBCC-chip problem, this board may be used in a graphics system only if it is the only processor board in the system.

030-0636-009: This revision used a new version of the Instruction Unit chip (P / N 098-0003-004) which eliminated the FastIU problem. It therefore did not need a thermostat control board or a chip heater. This board is functionally equivalent to 030-0636-109. Due to a BBCC-chip problem, this board may be used in a graphics system only if it is the only processor board in the system.

030-0702-002: This revision used the newer version of the BBCC chip, and is therefore suitable for use in either graphics or server systems

030-0703-002: This revision used the older version of the BBCC chip, and is therefore not suitable for use in a graphics system.

030-0858-001: This revision used the newer version of the BBCC chip, and is therefore suitable for use in either graphics or server systems.

Chapter 3

MC3 Memory Board Revision History

The MC3 memory board provides main memory for the Everest system. Each MC3 supports up to 2GB of RAM and is capable of performing both on-board and inter-board memory interleaving.

Note: The first revision of the MC3 board was limited to 1GB of RAM. See Section 3.1 for more information.

Each MC3 board has thirty-two 200-pin SIMM slots. The custom 200-pin SIMMs are available in either 16 Megabyte ('high density') or 64 Megabyte ('super density') capacities. The minimum MC3 configuration uses four 16 MB SIMMs and provides a total of 64 MB. The maximum MC3 configuration uses thirty-two 64 MB SIMMs and provides a total of 2 GB.

Typically at least two memory banks on each installed MC3 are populated (i.e., each board contains at least eight SIMMs). If the two banks are on different memory leaves they can be interleaved, producing a significant performance improvement. If a system uses two or four MC3 boards additional levels of interleaving can be obtained, further improving memory bandwidth. Configurations with three MC3 boards are not recommended because they greatly reduce memory-subsystem performance.

Note: For details about MC3 board configurations and memory interleaving see *CHALLENGE/Onyx L Deskside Installation Instructions* (SGI document number 108-7039-020), or *CHALLENGE/Onyx XL Rackmount Installation Instructions* (SGI document number 108-7042-020).

Different MC3 assembly numbers may mean that two boards are different. On the other hand, it may simply mean that the two boards were originally shipped with a different SIMM configuration, and the boards may be functionally equivalent.

There are three SIMM configurations with which a board may have been shipped:

- No SIMMs.
- Four 16 MB SIMMs (for a total of 64 MB).
- Four 64 MB SIMMs (for a total of 256 MB).

However the configuration of the board when shipped has no bearing on the configurations in which it may later be used, since SIMMs are often added by the customer.

Table 3-1Figure 3-1 lists the current part-number standards for MC3 board RAM configuration (note that these standards are relatively recent). When a board uses more than the minimum of four SIMMs additional kits of SIMMs may be shipped to account for the difference.

Assembly #	Shipped with	RAM Config.
030-0604-xxx	64 MB	4x16 MB
030-0613-xxx	256 MB	4x64 MB
030-0614-xxx	0 MB	none

Table 3-1 Current Shipping MC3 Board RAM Configurations

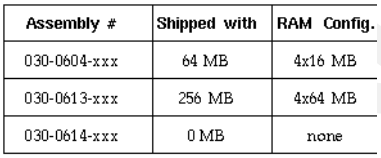

Figure 3-1 Current Shipping MC3 Board RAM Configurations

3.1 MC3 Board History

Due to problems with Memory Address (MA) ASIC version 2, the first revision of the MC3 board (030-0245-007) was only able to use sixteen of its thirty-two SIMM slots. Later MC3 boards (030-0245-008 and above) with version 3 or later of the MA ASIC supported the use of all thirty-two SIMM slots.

The 034-0245-003 FAB was found to have hold-time problems on some of the nets sourced by the MA ASIC. A small daughter-card was designed to fit between the MA ASIC and its socket on the MC3 board. This daughter-card, called the KL1-1, added a fixed amount of delay to the affected nets. KL1-1 cards were installed on 030-0245-010A, 030-0607-001A, and 030-0614-001A MC3 boards.

Later, the KL1-1 card was found to have problems, and was replaced with a KL1-2 card on 030-0607-001B MC3 boards. The KL1-2 card was subsequently replaced with a KL1-3 card on 030-0245-010B and 030-0607-002A MC3 boards.

In order to improve row-address hold time, six of the eight RAS delay lines were replaced on 030-0245-010B and 030-0607-002A MC3 boards. This change was made in order to eliminate certain memory errors.

A new FAB (034-0604-002B), making KL1 boards unnecessary, was released and used to create 030-0604-002A, 030-0607-001C, 030-0613-001B, 030-0614-001B and subsequent MC3 boards.

A three-pin header was added to the MC3 as of revision 030-0604-004. This header controls whether or not the MC3 interrupts the operating system when a correctable memory error occurs. At this revision level, the jumper is used primarily for diagnostic purposes. This revision is therefore of little significance for most applications.

A bug in the first version of the MD ASIC (099-0059-001), the version used on 030-0604-004 and earlier MC3 boards, allowed certain single-bit correctable errors in an MC3 board to reach the Ebus. This was corrected in the next version of the MD ASIC (099-0059-002), found on 030-0604-005, 030-0613-005, and 030-0614-005 and subsequent MC3 boards.

The old version of the MA ASIC (099-0052-003) was replaced with a newer version (099-0052-005) on 030-0604-006 MC3 boards. The new MA was able to report and log correctable errors (rather than halting the system). At this time a jumper was installed on the 3-pin header near the MA chip in order to activate the error-reporting that only the new MA was able to handle correctly.

A new FAB (034-0604-003), designed to reduce noise and incorporate a number of reworks, was released and used to create 030-0604-106, 030-0613-106, and 030-0614-106.

3.2 MC3 Indications for Use

All systems should have an absolute minimum revision level of 030-0245-008 of the MC3 board (the “Retrofit I” level). This allows them to use their entire thirty-two SIMM slots.

All systems should have at least 030-0245-010, 030-0607-001, or 030-0613-001 MC3 boards (the “Retrofit II” level*). These revisions contain a KL-1 daughterboard (located under the MA chip), and fix a number of system hang and system panic problems. Details may be found in *CHALLENGE and Onyx Retrofit II Requirements*.

When possible, systems should use MC3 boards based on the newer FABs (034-0604-002 or 034-0604-003). See Table 3-2Figure 3-2.

If a system is having problems using 64 MB (‘super density’) SIMMs, it should get any of the MC3 boards in Group 8 or later, Table 3-2Figure 3-2.

If a system is experiencing Ebus parity errors and system crashes, it should get any of the MC3 boards in Group 10 or later, Table 3-2Figure 3-2.

Figure 3-2 MC3 Board Functional Equivalencies

* For additional information see *CHALLENGE and Onyx Retrofit II Requirements*, SGI Document Number 802-0113-001.

Group	FAB 034-0245-003	FAB 034-0604-002	FAB 034-0604-003	When Indicated
1	030-0245-007			
2	030-0245-008			Retro. I Mi
3	030-0245-009			
4	030-0245-010A 030-0607-001A 030-0613-001A 030-0614-001A			Retro. II Mi
5	030-0607-001B			
6	030-0245-010B			
7		030-0604-002 030-0607-001C 030-0613-001B 030-0614-001B		
8		030-0607-001D 030-0613-001C 030-0614-001C 030-0613-002 030-0614-002 030-0604-003 030-0613-003 030-0614-003		Fixes 64 MI SIMM problems
9		030-0604-004 030-0613-004 030-0614-004		
10		030-0604-005 030-0613-005 030-0614-005		New MD A

Table 3-2 MC3 Board Functional Equivalencies

Group	FAB 034-0245-003	FAB 034-0604-002	FAB 034-0604-003	When Indicated
1	030-0245-007			
2	030-0245-008			Retro. I Min.
3	030-0245-009			
4	030-0245-010A 030-0607-001A 030-0613-001A 030-0614-001A			Retro. II Min.
5	030-0607-001B			
6	030-0245-010B			

Table 3-2 MC3 Board Functional Equivalencies

7		030-0604-002 030-0607-001C 030-0613-001B 030-0614-001B		
8		030-0607-001D 030-0613-001C 030-0614-001C 030-0613-002 030-0614-002 030-0604-003 030-0613-003 030-0614-003		Fixes 64 MB SIMM problems
9		030-0604-004 030-0613-004 030-0614-004		
10		030-0604-005 030-0613-005 030-0614-005		New MD ASIC
11		030-0604-006 030-0613-006 030-0614-006	030-0604-106 030-0613-106 030-0614-106	New MA ASIC

3.3 MC3 Board Revisions

030-0245-007: This was the first version of the MC3 to ship, and is based on the 034-0245-003B FAB. This revision of the MC3 could use only sixteen of its thirty-two SIMM slots. It is also incompatible with all but the earliest IP19 boards. For these reasons, and others, this revision should no longer be in use in the field.

030-0245-008A: This revision of the MC3 replaced revision 2 of the MA ASIC (099-0052-002) with revision 3 (099-0052-003), allowing the board to use the upper sixteen of its thirty-two SIMM slots (i.e., address a full 2 GB of RAM). Note that the IP19 PROM must also change in order to use this memory (details may be found in the IP19 section). Due to a number of compatibility and reliability issues, this revision should no longer be in use in the field.

030-0245-008B: This revision changes from one type of socket to another to allow the use of plastic-packaged ASICs. It is functionally equivalent to 030-0245-008A. Due to a number of compatibility and reliability issues, this revision should no longer be in use in the field.

030-0245-009: This revision added wires to connect all MA and MD PLL V_{SS}IN pins to ground in order to reduce noise and clock jitter. Due to a number of compatibility and reliability issues, this revision should no longer be in use in the field.

030-0245-010A: This revision added a KL1-1 board under the MA ASIC in an attempt to solve hold-time problems found on all of the early 034-0245-003 FABs. Also, in an attempt

to reduce noise and clock jitter at the 5 MC3 ASICs, it removed the MA heatsink and socket, removed the wires added in revision 030-0245-009 (they were found to make the noise and jitter problems worse), added a resistive power jumper (P / N 9093305, 120K Ohms: reduces V_{CC} from +5.0V to +4.9V), and made a number of smaller changes. Except for differences in SIMM quantities, this revision is the same as 030-0607-001A, 030-0613-001A, 030-0614-001A.

030-0245-010B: This revision replaced the KL1-1 with a KL1-3 and changed six of the eight RAS delay lines in order to improve row-address hold-time.

030-0578-001A: This revision is based on the 034-0245-003B FAB (in spite of the base-number change). It replaced the MA ASIC's 299-pin socket with a custom 298-pin socket (essentially a 299-pin socket with one pin removed). Records indicate that this revision was never shipped to the field. [Note: The ECO for this revision is unavailable. This entry is therefore based on other sources of information, which may be less reliable.]

030-0607-001A: Except for differences in SIMM quantities, this revision is equivalent to 030-0245-010A. See listing above for details. Records indicate that this revision was never shipped to the field.

030-0607-001B: This revision replaces the KL1-1 board (030-0598-001) with a KL1-2 board (030-0598-002). Records indicate that this revision was never shipped to the field.

030-0607-001C: This revision of the MC3 board is based on the 034-0604-002 FAB, and was initially shipped with four 16 MB SIMMs (for a total of 64 MB).

030-0607-001D: This revision changed six of the eight RAS delay lines in order to improve row-address hold-time. After this revision, the 030-0607-xxx line was replaced by the 030-0604-xxx line.

030-0604-001: This revision was a prototype, and was never shipped.

030-0604-002A: This revision, like all 030-0604-xxx MC3 boards, is based on the 034-0604-002 FAB. It was superseded at the same time it was released, so it is likely that none were shipped.

030-0604-003A: This revision changed six of the eight RAS delay lines in order to improve row-address hold-time. This revision (or later) is necessary in order for the MC3 board to work properly with 64 MB SIMMs. At this point in the series, the 030-0604-xxx line replaced the 030-0607-xxx line.

030-0604-004A: This revision installed a MEM_ERR_OD[0] 3-pin header at location G2B7 and changed to a different style of daughter-card connectors. At this revision level, the 3-pin header was only used for diagnostic purposes. With a jumper in place, certain correctable errors would halt the system. The jumper was therefore not left in place during normal operation.

030-0604-005A: This revision replaced all four of the version A MD ASICs (099-0059-001) with version B MD ASICs (099-0059-002). This eliminated a problem in which certain correctable single-bit parity errors on the MC3 caused Ebus parity errors and system crashes.

030-0604-006A: This revision replaced version 3 of the MA ASIC (099-0052-003) with version 5 (099-0052-005), allowing the MA to correctly report and log correctable errors (rather than halting the system). This revision also added a jumper between pins 1 and 2 of the 3-pin header at location G2B7 (the two pins farthest from the MA ASIC). The jumper enables reporting of single-bit errors. This revision is functionally equivalent to 030-0604-006B, 030-0604-006C, and 030-0604-106A.

030-0604-006B: This revision is simply a BOM correction. It is functionally equivalent to 030-0604-006A, 030-0604-006C, and 030-0604-106A.

030-0604-006C: This revision removed a number of PGA sockets from the MC3 board. At the same time, it was necessary to change the heatsinks from clip-on to stick-on. This revision is functionally equivalent to 030-0604-006A, 030-0604-006B, and 030-0604-106A.

030-0604-106A: This revision is based on the 034-0604-003 FAB. It is functionally equivalent to 030-0604-006A, 030-0604-006B, and 030-0604-006C.

030-0607-xxx: These boards are listed before the 030-0604-xxx boards, since they came first chronologically.

030-0613-001A: Except for a difference in SIMM quantities, this revision is equivalent to 030-0245-010A and 030-0614-001A, and uses the older FAB (034-0245-003B). See the description under 030-0245-010A (above) for details. Records indicate that this revision was never shipped to the field. Table 3-1Figure 3-1 indicates the SIMM configurations this would have had if any did ship. Note that this revision is *not* equivalent to 030-0604-001.

030-0613-001B: This revision of the MC3 board is based on the 034-0604-002 FAB. This and all subsequent revisions do not use the KL1 board. Aside from a difference in SIMM configuration at shipment (see Table 3-1Figure 3-1 for details), this revision is equivalent to 030-0614-001B. Note that this revision is *not* equivalent to 030-0604-001.

030-0613-001C: This revision changed six of the eight RAS delay lines in order to improve row-address hold-time. Aside from a difference in SIMM configuration at shipment (see Table 3-1Figure 3-1 for details), this revision is equivalent to 030-0614-001C. Note that this revision is *not* equivalent to 030-0604-001.

030-0613-002A: This revision simply represents a dash-number change. It was found that the previous revision was necessary in order for the MC3 board to work properly with 64 MB SIMMs. It was decided that this difference deserved a full dash-number change, rather than simply a new letter. Aside from a difference in SIMM configuration at shipment (see Table 3-1Figure 3-1 for details), this revision is equivalent to 030-0614-002A. Note that this revision is *not* equivalent to 030-0604-002.

030-0613-003A: This revision simply represents another dash-number change. Some 030-0613-002A and 030-0614-002A boards were found to not have the RAS delay lines which were supposed to have been added in revision 030-0613-001C and 030-0614-001C. In addition, the 030-0613-xxx and 030-0614-xxx board revision numbers were out of synchronization with the 030-0604-xxx board revision numbers. This number change brings them all back into synch. Except for the difference in SIMM configuration at time of shipment (see Table 3-1Figure 3-1 for details), this revision is equivalent to 030-0604-003A and 030-0614-003A.

030-0613-004A: See the description under 030-0604-004A for details of this revision. Aside from a difference in the SIMM configuration at time of shipment (see Table 3-1Figure 3-1 for details) this revision is equivalent to 030-0604-004A and 030-0614-004A.

030-0613-005A: See the description under 030-0604-005A for details of this revision. Aside from a difference in the SIMM configuration at time of shipment (see Table 3-1Figure 3-1 for details) this revision is equivalent to 030-0604-005A and 030-0614-005A.

030-0613-006A: See the description under 030-0604-006A for details of this revision. Aside from a difference in the SIMM configuration at time of shipment (see Table 3-1Figure 3-1 for details) this revision is equivalent to 030-0604-006A and 030-0614-006A.

030-0613-006B: See the description under 030-0604-006B for details of this revision. Aside from a difference in the SIMM configuration at time of shipment (see Table 3-1Figure 3-1 for details) this revision is equivalent to 030-0604-006B and 030-0614-006B.

030-0613-006C: See the description under 030-0604-006C for details of this revision. Aside from a difference in the SIMM configuration at time of shipment (see Table 3-1Figure 3-1 for details) this revision is equivalent to 030-0604-006C and 030-0614-006C.

030-0613-106A: See the description under 030-0604-106A for details of this revision. Aside from a difference in the SIMM configuration at time of shipment (see Table 3-1Figure 3-1 for details) this revision is equivalent to 030-0604-106A and 030-0614-106A.

030-0614-001A: Except for a difference in SIMM quantities, this revision is equivalent to 030-0245-010A and 030-0613-001A, and uses the older FAB (034-0245-003B). See the description under 030-0245-010A (above) for details. Records indicate that this revision was never shipped to the field. Table 3-1Figure 3-1 indicates the SIMM configurations this would have had if any did ship. Note that this revision is *not* equivalent to 030-0604-001.

030-0614-001B: This revision of the MC3 board is based on the 034-0604-002 FAB. This and all subsequent revisions do not use the KL1 board. Aside from a difference in SIMM configuration at shipment (see Table 3-1Figure 3-1 for details), this revision is equivalent to 030-0613-001B. Note that this revision is *not* equivalent to 030-0604-001.

030-0614-001C: This revision changed six of the eight RAS delay lines in order to improve row-address hold-time. Aside from a difference in SIMM configuration at shipment (see Table 3-1Figure 3-1 for details), this revision is equivalent to 030-0613-001C. Note that this revision is *not* equivalent to 030-0604-001.

030-0614-002A: This revision simply represents a dash-number change. It was found that the previous revision was necessary in order for the MC3 board to work properly with 64 MB SIMMs. It was decided that this difference deserved a full dash-number change, rather than simply a new letter. Aside from a difference in SIMM configuration at shipment (see Table 3-1Figure 3-1 for details), this revision is equivalent to 030-0613-002A. Note that this revision is *not* equivalent to 030-0604-002.

030-0614-003A: This revision simply represents another dash-number change. Some 030-0613-002A and 030-0614-002A boards were found to not have the RAS delay lines which were supposed to have been added in revision 030-0613-001C and 030-0614-001C. In addition, the 030-0613-xxx and 030-0614-xxx board revision numbers were out of synchronization with the 030-0604-xxx board revision numbers. This number change

brings them all back into synch. Aside from a difference in SIMM configuration at shipment (see Table 3-1Figure 3-1 for details), this revision is equivalent to 030-0604-003A and 030-0613-003A.

030-0614-004A: See the description under 030-0604-004A for details of this revision. Aside from a difference in the SIMM configuration at time of shipment (see Table 3-1Figure 3-1 for details) this revision is equivalent to 030-0604-004A and 030-0613-004A.

030-0614-005A: See the description under 030-0604-005A for details of this revision. Aside from a difference in the SIMM configuration at time of shipment (see Table 3-1Figure 3-1 for details) this revision is equivalent to 030-0604-005A and 030-0613-005A.

030-0614-006A: See the description under 030-0604-006A for details of this revision. Aside from a difference in the SIMM configuration at time of shipment (see Table 3-1Figure 3-1 for details) this revision is equivalent to 030-0604-006A and 030-0613-006A.

030-0614-006B: See the description under 030-0604-006B for details of this revision. Aside from a difference in the SIMM configuration at time of shipment (see Table 3-1Figure 3-1 for details) this revision is equivalent to 030-0604-006B and 030-0613-006B.

030-0614-006C: See the description under 030-0604-006C for details of this revision. Aside from a difference in the SIMM configuration at time of shipment (see Table 3-1Figure 3-1 for details) this revision is equivalent to 030-0604-006C and 030-0613-006C.

030-0614-106A: See the description under 030-0604-106A for details of this revision. Aside from a difference in the SIMM configuration at time of shipment (see Table 3-1Figure 3-1 for details) this revision is equivalent to 030-0604-106A and 030-0613-106A.

Chapter 4

IO4 Input/Output Board Revision History

The IO4 board, sometimes referred to as the POWERchannel-2 board, performs a more varied set of tasks than any other board in the Everest system. There can be between one and four IO4 boards in a rack system (and between one and three in a deskside system). The first IO4 in a system:

- Maintains an NVRAM for storage of system configuration information.
- Maintains the second-level boot Flash PROM.
- Provides an interface for up to 8 SCSI buses (with a total of up to 120 SCSI devices).
- Provides an interface to ethernet.
- Provides an interface to a VME64 bus.
- Provides an FCI (Flat Cable Interconnect) interface for the connection of a graphics board set.
- Provides connections for external serial (RS-232 & RS-422) and parallel devices, system interrupt, and keyboard.
- Contains the system's time-of-day clock.
- Provides two Ibus ("mezzanine") connectors for SGI or third-party add-on cards.

Each additional IO4 board can supply four more Ibus connectors, usable for additional graphics board sets, VME64 interfaces, or other SGI or third-party add-on cards.

Table 4-1Figure 4-2 lists the revisions of the IO4 board, and separates them into five equivalence classes (as indicated by the numbers in the left column of the table). With one notable exception, explained below, any board in a particular row is functionally equivalent to any other board in that row.

4.1 IO4 Board History

The most significant changes made to the IO4 line came with the 034-0377-003 FAB. This new FAB implemented two changes: the addition of a +12V supply to the mezzanine connectors and the addition of support for a dual-hosted SCSI bus. In honor of this change, the IO4 got a new base number (making it 030-0646-xxx), and a new name (it is officially called the "IO4B").

Note: There are, as of yet, no mezzanine cards requiring the +12V supply (its inclusion is for future products), and dual-hosted SCSI capability is needed only in applications requiring the ability to have two Everest systems connected to the same SCSI bus (these would typically be fault-tolerant systems).

With the exception of the above distinction, a board within a row of Table 4-1Figure 4-2 is functionally equivalent to any other board in that row, and it is unimportant which column a board is from.

The newest FAB, 034-0646-001, incorporates no functional changes compared to earlier FABs. This FAB spin was simply required due to the unavailability of map-RAM chips from the original supplier. The use of this newer FAB is indicated by a "1" in the first digit of the dash number for the PCA (i.e., 030-0646-1xx). In order to make it easier to keep track of functionally equivalent assemblies, the -1xx series started at 030-0646-103, which is functionally equivalent to 030-0646-003. Later revisions of these boards continue in this manner (i.e., 030-0646-104 is functionally equivalent to 030-0646-004). For all practical purposes it would be reasonable to simply ignore the "1" in the first digit of the dash number.

Table 4-1Figure 4-2 shows which FABs each IO4 board is based on. Note that the 030-0377-006 through 030-0377-009 IO4 boards may be based on either the 034-0240-005 FAB or the 034-0377-002 FAB. This can be a point of confusion in dealing with IO4 boards.

4.2 IO4 Indications for Use

Group 1 (in Table 4-1Figure 4-2) is included only for historical purposes. These boards should no longer be in use in the field.

Regardless of configuration, all systems in the field should use IO4 boards at the "Retrofit II" level, which are generally those in Group 2 or later. In some cases, if a system is running without trouble, Retro. II allows the use of 030-0240-011 and 030-0240-012 (from Group 1).

030-0377-003 and 030-0377-004 have serial-port problems. For this reason, it is recommended that these boards be replaced with 030-0377-005 or later boards.

If a system is having ethernet problems, contains an Efast board, or has other unusual ethernet requirements, all IO4 boards used should be from those listed in Group 3 or later.

The first revision of the Flash PROM to support IP21 processor boards was version 3.04. This is found in 030-0377-008 and in 030-0646-x03 and later IO4 boards. Systems containing IP21 processor boards therefore require IO4 boards from Groups 4 or 5.

Rack systems containing IP21 processor boards require the use of either of the IO4 boards listed in Group 5.

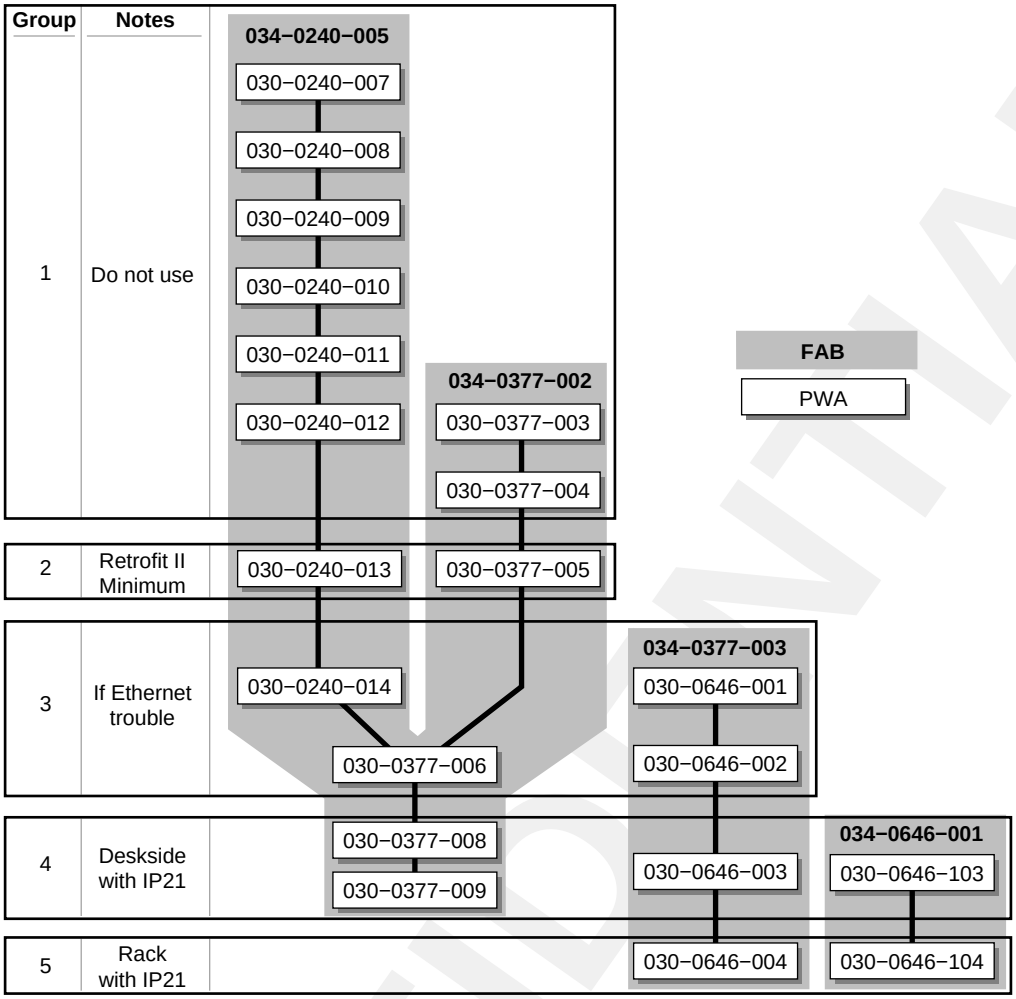

Figure 4-1 IO4 History Diagram

Figure 4-2 IO4 Board Functional Equivalencies

Group	FAB 034-0240-005	FAB 034-0377-002	FAB 034-0377-003	FAB 034-0646-001	When Indicated
1	030-0240-007				Obsolete
	030-0240-008				
	030-0240-009				
	030-0240-010				
	030-0240-011				
	030-0240-012	030-0377-003[a]			
2	030-0240-013	030-0377-004[a] 030-0377-005			Retro. II Min.
3	030-0240-014 030-0377-006	030-0377-006	030-0646-001 030-0646-002		If Enet trouble
4	030-0377-008 030-0377-009	030-0377-008 030-0377-009	030-0646-003	030-0646-103	Desk w/ IP21
5			030-0646-004	030-0646-104	Rack w/ IP21
Shaded boards have 12V supply to mezz. connectors & dual-hosted SCSI. All others do not.					

a. See warning in Section 4.2 about these boards.

Table 4-1 IO4 Board Functional Equivalencies

Group	FAB 034-0240-005	FAB 034-0377-002	FAB 034-0377-003	FAB 034-0646-001	When Indicated
1	030-0240-007				Obsolete
	030-0240-008				
	030-0240-009				
	030-0240-010				
	030-0240-011				
	030-0240-012	030-0377-003[a]			
2	030-0240-013	030-0377-004[a] 030-0377-005			Retro. II Min.
3	030-0240-014 030-0377-006	030-0377-006	030-0646-001 030-0646-002		If Enet trouble
4	030-0377-008 030-0377-009	030-0377-008 030-0377-009	030-0646-003	030-0646-103	Desk w / IP21
5			030-0646-004	030-0646-104	Rack w / IP21
Shaded boards have 12V supply to mezz. connectors & dual-hosted SCSI. All others do not.					

a. See warning in Section 4.2 about these boards.

4.3 IO4 Board Revisions

030-0240-007: This was the first version of the IO4 to ship. Due to a number of compatibility and reliability issues, this revision should no longer be in use in the field.

030-0240-008A: This revision removed an incorrect connection from one of the EPC pins. Due to a number of compatibility and reliability issues, this revision should no longer be in use in the field.

030-0240-008B: This revision reduced the value of the pull-up resistor on one of the SCSI controller signal lines. This improved the SCSI controller's response time, thus making the SCSI buses more reliable. Due to a number of compatibility and reliability issues, this revision should no longer be in use in the field.

030-0240-009: This revision added pull-up resistors to two of the EPC's interrupt sources (eliminating spurious interrupts) and modified the Centronics parallel port (making pin 17 bidirectional). Due to a number of compatibility and reliability issues, this revision should no longer be in use in the field.

030-0240-010: This revision added a previously-missing ground wire and performed 3 PAL changes. Due to a number of compatibility and reliability issues, this revision should no longer be in use in the field.

030-0240-011: This revision replaced the TXRBLK PAL with one containing slightly different equations, correcting a problem found when using 10ns 22V10 PALs (the problem never showed up with the original 15ns 22V10 PALs). In addition, the output enable for the RS-422 driver was corrected to be pulled-down instead of pulled-up. Due to a number of compatibility and reliability issues, this revision should no longer be in use in the field. This revision is functionally equivalent to 030-0377-002, except that 030-0377-002 has a serious serial-port problem.

030-0240-012: This revision replaced one of the two F1 ASICs with an F2 ASIC. The only FCI master able to take advantage of the improved performance of the F2 ASIC is the GFX on the GE10. In addition, this revision replaced the Level One LXT901 ethernet controller with a Level One ST10020PC ethernet controller. The ST10020PC was less sensitive to jitter in the data stream caused by certain transceivers. Finally, this revision used version H of the WD33C95A SCSI controller. Due to a number of compatibility and reliability issues, this revision should no longer be in use in the field. This revision is functionally equivalent to 030-0377-003, except that 030-0377-003 has a serious serial-port problem.

030-0240-013: This revision added a PAL to fix a problem with the ST10020PC ethernet controller. This is the lowest revision based on the 034-0240-005 FAB recommended for use in the field. This revision is functionally equivalent to 030-0377-004 and 030-0377-005, except that 030-0377-004 has a serious serial-port problem.

030-0240-014: This revision replaces the ethernet controller's clock crystal with a more reliable clock oscillator output, improving the IO4's ethernet functionality. This revision is therefore recommended for systems with ethernet problems or unusual ethernet requirements (such as the use of an Efast board). This revision is functionally equivalent to 030-0377-006, 030-0646-001*, and 030-0646-002*.

030-0377-001: This part number was used for an engineering prototype board. It was never a shipping part.

030-0377-002: This part number was not used.

030-0377-003: This revision replaces one of the two F1 ASICs with an F2 ASIC. The only FCI master able to take advantage of the improved performance of the F2 ASIC is the GFX on the GE10. In addition, this revision replaces the Level One LXT901 ethernet controller with a Level One ST10020PC ethernet controller. The ST10020PC is less sensitive to jitter in the data stream caused by certain transceivers. Due to serial-port-controller problems (excessive noise on the PBus write strobe) this revision should not be in use in the field. Aside from this board's serial-port problems, however, it is functionally equivalent to 030-0240-012. This board was superseded by the 030-0377-004 revision before shipping, so it is unlikely that many will be seen in the field.

030-0377-004: This is the first shipping version of the IO4 based on the 034-0377-002 FAB. This revision added pull-up resistors to the EPC's interrupt sources, eliminating spurious interrupts from the serial-port controllers and the real-time clock. It also modifies the Centronics parallel port (making pin 17 bidirectional). Due to serial-port-controller problems (excessive noise on the PBus write strobe) this revision should not be in use in the field. Aside from this board's serial-port problems, however, it is functionally equivalent to 030-0240-013.

030-0377-005: This revision replaces a 74ALS244 with a 74F244. The new part significantly improves the noise characteristics of the PBus write strobe, which in turn improves the reliability of the Zilog serial-port controllers. This change is only necessary on boards based on the 034-0377-002 FAB. This revision is functionally equivalent to 030-0240-013, and is the lowest 034-0377-002-FAB-based revision recommended for use in the field.

030-0377-006: This revision replaces the ethernet controller's clock crystal with a more reliable clock oscillator output, improving the IO4's ethernet functionality. This revision is therefore recommended for systems with ethernet problems or unusual ethernet requirements (such as the use of an Efast board). This revision is functionally equivalent to 030-0240-014, 030-0646-001*, and 030-0646-002*.

030-0377-007: This part number was used for the engineering prototype of 030-0646-001. It was never a shipping part.

030-0377-008: This revision reprograms the Flash PROM to a minimum of version 3.04. Version 3.04 of the PROM is the first to support IP21 processor boards, therefore systems containing IP21 processor boards should use at least this revision of the IO4 board. This revision is functionally equivalent to 030-0377-009, 030-0646-003*, and 030-0646-103*.

030-0377-009: This revision replaces the Level One ST10020PC ethernet controller (which became unavailable) and its associated PAL with the new Level One LXT907 ethernet

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* Except for the fact that 030-0646-xxx IO4 boards have 12V supply to the mezzanine cards and dual hosted SCSI support.

* Except for the fact that 030-0646-xxx IO4 boards have 12V supply to the mezzanine cards and dual hosted SCSI support.

controller (which doesn't need a PAL). This replacement did not change the functional characteristics of the board. This revision is functionally equivalent to 030-0377-008, 030-0646-003*, and 030-0646-103*.

030-0646-001: This is the first revision of the IO4 based on the 034-0377-003 FAB. Aside from its 12V supply to the mezzanine cards and its support for dual-hosted SCSI, this revision is functionally equivalent to 030-0240-014 and 030-0377-006. This revision is fully functionally equivalent to 030-0646-002.

030-0646-002: This revision replaces the Level One ST10020PC ethernet controller (which became unavailable) and its associated PAL with the new Level One LXT907 ethernet controller (which doesn't need a PAL). This replacement did not change the functional characteristics of the board. Aside from its 12V supply to the mezzanine cards and its support for dual-hosted SCSI, this revision is functionally equivalent to 030-0240-014 and 030-0377-006. This revision is fully functionally equivalent to 030-0646-001.

030-0646-003: This revision guarantees a minimum Flash PROM level of 3.04. Version 3.04 of the PROM is the first to support IP21 processor boards, therefore systems containing IP21 processor boards should use at least this revision of the IO4 board. Aside from its 12V supply to the mezzanine cards and its support for dual-hosted SCSI, this revision is functionally equivalent to 030-0377-008 and 030-0377-009. This revision is fully functionally equivalent to 030-0646-103.

030-0646-004: This revision replaces EPC ASIC part number 099-0054-002 with EPC ASIC part number 099-0054-003. This new EPC is required to support configurations with a large number of IP21 processor boards, which can only be found in heavily loaded rack Power CHALLENGE systems. This revision is functionally equivalent to 030-0646-104.

030-0646-103: This revision reprograms the Flash PROM to a minimum revision level of 3.04. Version 3.04 of the PROM is the first to support IP21 processor boards, therefore systems containing IP21 processor boards should use at least this revision of the IO4 board. Aside from its 12V supply to the mezzanine cards and its support for dual-hosted SCSI, this revision is functionally equivalent to 030-0377-008 and 030-0377-009. This revision is fully functionally equivalent to 030-0646-003.

030-0646-104: This revision replaces EPC ASIC part number 099-0054-002 with EPC ASIC part number 099-0054-003. This new EPC is required to support configurations with a large number of IP21 processor boards, which can only be found in heavily-loaded rack Power CHALLENGE systems. This revision is functionally equivalent to 030-0646-004.

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