IRIS® HIPPI Installation Instructions

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Contributors

Written by Carlin Otto
Illustrated by Dan Young, Carlin Otto, and Cheri Brown
Edited by Ann Wood
Production by Julia Lin
Engineering contributions by Ken Powell and Thomas Skibo

IRIS HIPPI Installation Instructions
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Silicon Graphics, Inc.
Mountain View, California

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Introduction

The IRIS® HIPPI product is a network interface controller (hardware) and driver (software) providing data communication with the High-Performance Parallel Interface (HIPPI). The product provides HIPPI connectivity for CHALLENGE™ L and XL and Onyx™ platforms.

For networking, IRIS HIPPI supports TCP/IP over HIPPI-LE in conformance with RFC 1374 guidelines.

IRIS HIPPI provides an application programming interface (API) that customers can use to develop their own upper-layer applications (ULPs). Customer-developed ULPs can be designed to coexist with IRIS HIPPI's HIPPI-LE ULP module. See the *IRIS HIPPI API Programmer's Guide* (shipped with each IRIS HIPPI board) for details about developing upper-layer applications.

The IRIS HIPPI hardware must be installed by a Silicon Graphics system support engineer (SSE) or other person trained by Silicon Graphics in installation procedures. This document, *IRIS HIPPI Installation Instructions,* is provided to each SSE and contains complete details for hardware installation.

Installation and configuration of the software can be done by customers and/or SSEs. The *IRIS HIPPI Administrator's Guide* (shipped with each IRIS HIPPI board) provides software configuration details. The online *IRIS HIPPI Release Notes* provide software installation instructions.

Standards Based

The IRIS HIPPI network product adheres to the ANSI standards listed below, thus ensuring successful interoperability with other HIPPI equipment that is standards-compliant:

- HIPPI-PH: X3.183-1991
- HIPPI-SC: X3.222-1993
- HIPPI-FP: X3.210-1992
- HIPPI-LE: X3.218-1993

Application Programming Interface

The IRIS HIPPI product includes an application programming interface (API) that allows customer-developed upper layer applications to control the IRIS HIPPI subsystem. The API is a character device interface. This interface is described in the *IRIS HIPPI API Programmer's Guide* that is shipped with each IRIS HIPPI board.

On-board Intelligence

The IRIS HIPPI board has an AMD 29030 CPU that handles protocol processing and channel control. The board contains logic for handling transport layer (TCP and UDP) checksumming on both transmission and reception. These features provide two advantages: they increase the rate of data throughput for the board and free the host system's CPUs for work on user application tasks.

Chapter 1

Some HIPPI Basics

This chapter is an introduction to the High-Performance Parallel Interface (HIPPI) protocol and the IRIS HIPPI hardware. The chapter provides a brief introduction to HIPPI, a description of the HIPPI protocol, some common configurations of HIPPI equipment, how to obtain official HIPPI documentation, and a theory of operations section for the IRIS HIPPI hardware.

1.1 Introduction to the HIPPI Protocol

This section provides a brief introduction to HIPPI.

1.1.1 HIPPI Terminology

HIPPI uses *source* to refer to the transmitting host, endpoint, network interface, or program.

It uses *destination* to refer to the receiving host, endpoint, network interface, or program.

1.1.2 How HIPPI Works

HIPPI is an extremely fast, simplex point-to-point protocol. HIPPI provides for transmission at 800 or 1600 megabits per second*. Before data can be sent from one HIPPI network interface (endpoint) to another there must be both a physical link and an open connection between them. The physical link is made up of one or more 25-meter sections of copper cable. Each section connects two HIPPI nodes. The nodes can be endpoints or intermediate HIPPI switches. The open connection is an agreement for data transfer from one endpoint to another, and is arranged with an exchange of signals. Once a connection is open the entire physical link is dedicated to one-way communication from the source to the destination.

* IRIS HIPPI supports only 800 Mbits per second.

Figure 1-1 illustrates a configuration of HIPPI equipment with six physical links. This configuration supports nine different endpoint-to-endpoint communication paths (listed below) of which three can be simultaneously active:

- A-source transmitting to C-destination, B-destination, or A-destination (itself)
- B-source transmitting to C-destination, B-destination (itself), or A-destination
- C-source transmitting to C-destination (itself), B-destination, or A-destination

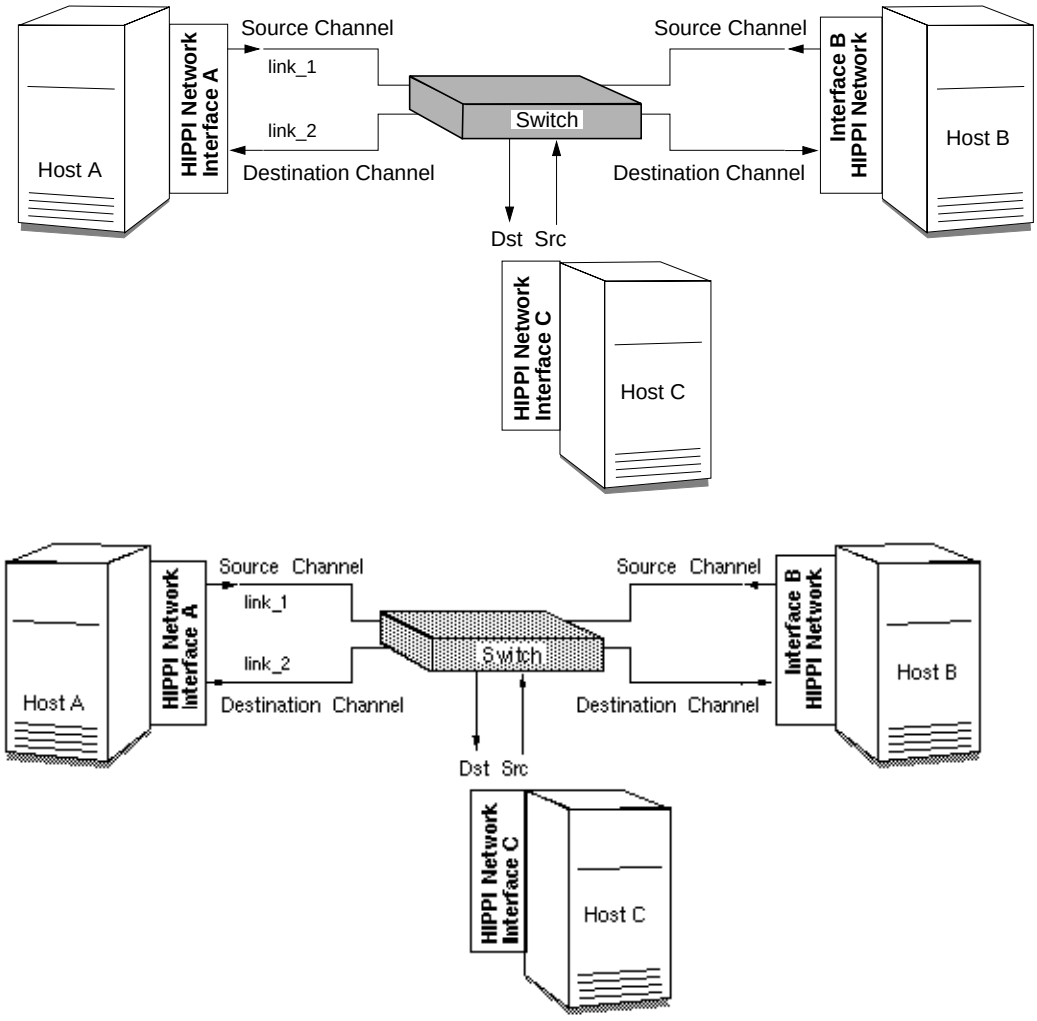

Figure 1-1 HIPPI Links and Connections

An open connection consists of an exchange of signals between a source and a destination. During this exchange, the destination agrees to accept data exclusively from the source. Each endpoint-to-endpoint link supports one connection (that is, HIPPI is point to point). It is common for an interface's source and destination channels to have open connections with different hosts (for example, A-source connected to B-destination while A-destination is connected to C-source). To move data in both directions between two hosts, two endpoint-to-endpoint links and two open connections are needed between the two hosts.

Unlike Ethernet, 802.5 Token Ring, or FDDI, HIPPI does not use a shared medium. Once a connection is established, the cable between the two HIPPI interfaces contains only packets transmitted by the source (that is, HIPPI connections are simplex). HIPPI packets may be seen by intermediate switches but not by other host interfaces. When one packet has been sent, the connection may be closed or kept open so that additional packets can be sent; however, each endpoint may not participate in another connection until the current one has been closed.

HIPPI communication is controlled by three basic functions: connection control, packet and flow control, and routing control (pertinent only when one or more switches are involved). Each of these is discussed separately in the subsections that follow.

1.1.3 Connection Control

One of the first things any HIPPI endpoint does upon startup is to assert its two outgoing **INTERCONNECT** signals and to look for assertion of its two incoming **INTERCONNECT** signals. Each channel (the source and the destination) has both incoming and outgoing **INTERCONNECT** signals. When both signals on a channel are asserted, the physical link between the local system and the system at the other end is ready for use. When the other system is a switch, the exchange of **INTERCONNECT** signals occurs between the endpoint and the switch, not between endpoints.

Before a source (transmitting) HIPPI network interface can send a packet, it must open a connection to one destination HIPPI endpoint. The source interface is always the initiator for opening the connection. To open a connection, the sender issues a connection request by asserting the **REQUEST** signal on the link. Each connection request includes an I-field (described in Section 1.2.1). The I-field mainly contains routing information, used by any switches encountered along the path to the destination.

The destination accepts a connection by asserting its `CONNECT` signal in response to the request. If the destination endpoint is unwilling to accept the connection or if there is a problem with the connection request (for example, bad parity on the I-field or incompatible word size), the connection request is denied (that is, acknowledged, then rejected). The transmitter must wait and try again later or forgo the communication. If the destination is unreachable (for example, a broken physical link, a powered-down or dysfunctional network interface), there is no response and the source program times out.

When a switch exists between the source and destination, the source receives its connection rejections from the switch, not directly from the destination. The rejection can be caused by any of the following conditions, and it is not possible to distinguish among them (except as explained below):

1. the destination is malfunctioning
2. the destination refuses to accept the requested connection
3. the connection request has an error
4. a section of the physical link to the destination is busy (currently engaged in another connection)

A feature is available that allows the source to be informed of rejections due to error conditions (items 1-3 above) but not to be informed (bothered) when the rejection is due to

a busy link (item 4). This feature is called *camp-on*. By setting the camp-on bit in the I-field, the source can program the switches to hold onto the connection request until the busy link to the destination becomes available.

When the Camp-on bit is set, the first switch enqueues the connection request if it finds any link along the path to the destination busy. The switch periodically checks to see if the link has become available. When the link becomes available, it sends the connection request. A switch will continue to wait until it sends the **REQUEST** to the ultimate destination endpoint or until the source aborts the connection request. If a number of sources are all trying to send data through the same link, the camp-on feature ensures fair (first come, first served) access to the link.

Once opened, a HIPPI connection may be kept open for as long as the two endpoints maintain it. Either endpoint may terminate the connection at any point in time; however, the source network interface is usually the initiator.

1.1.4 Packet Control (Data Flow)

Once a connection is open, one or multiple packets may be sent. The destination indicates it is ready to receive data by sending a READY signal to the source endpoint. Each READY allows the source to transmit one HIPPI *burst* (as explained below). All HIPPI source endpoints are required to be capable of enqueuing a minimum of 63 READYs. There is no minimum requirement for a destination's ability to generate READYs*. By sending ahead and queuing READYs, the two endpoints can optimize the throughput on their connection.

The source delineates its packets with the **PACKET** signal: at the beginning it asserts the **PACKET** signal, and at the end it deasserts the signal. A HIPPI packet consists of one or more bursts, as illustrated in Figure 1-2. Each burst contains 256 words, except in the case where the burst is *short* (as described below). The size of each word depends on the source's data bus (32 or 64 bits, as indicated by a bit in the I-field)†. At the end of each burst, the source generates a checksum (LLRC) so that the destination can detect any errors in the received data; in addition, each word has four bits of parity for error checking.

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* The source channel on the IRIS HIPPI board can enqueue up to 65,535 READYs; the destination channel can generate up to 255 outstanding READYs.

† The IRIS HIPPI board supports 32-bit words only.

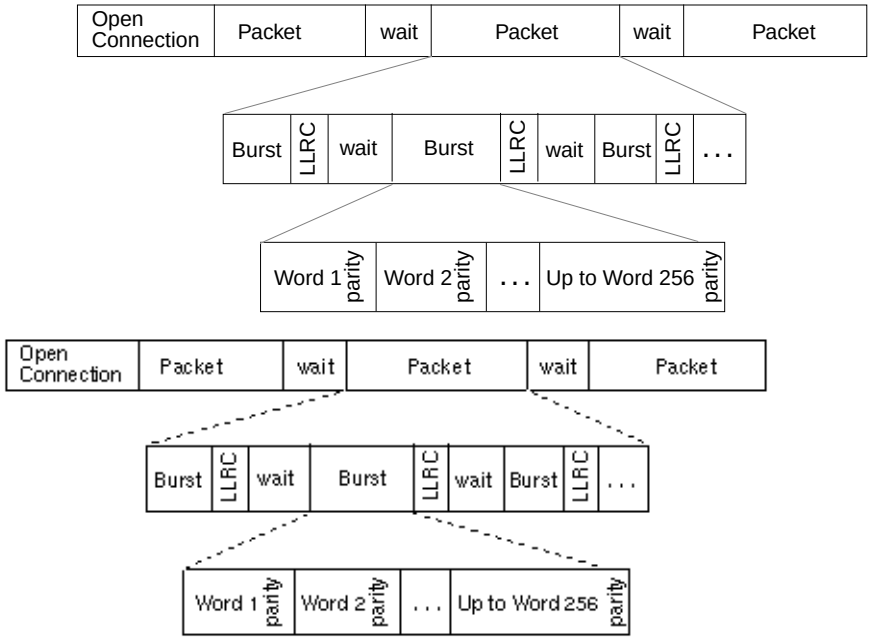


Figure 1-2 HIPPI Packets and Bursts

The HIPPI protocol requires very small waiting periods between packets and between bursts. These required periods are counted in nanoseconds and are essentially imperceptible to the user; however, in normal operation there may be noticeable pauses between bursts (for example, when the source is waiting to receive a READY).

As long as the source has READYs, it can transmit data as fast as it is capable of transmitting (but no faster than the protocol allows: 25 million words per second). When the sender has sent all the data for one packet, it indicates the end of the packet, using the PACKET signal. Indicating the end of the packet is necessary because HIPPI allows packet size to be undefined (indeterminate) at the start of the packet. A sender could essentially send an infinite-sized packet by keeping the PACKET signal asserted at all times.

A packet's first burst often contains some kind of header (for example, a HIPPI-FP header as described in Section 1.2). The first burst can contain header only or header and user data. In other words, the first words of user data can be in the first burst or the second. If the source program is generating HIPPI-FP packets, it can indicate the location of the packet's first word of user data by setting the B bit in the HIPPI-FP header.

Either the first or the last burst of a packet (but not both) can be less than 256 words. This burst is referred to as a *short* burst. Usually, the last burst is the short one. When the first burst is the short one, it contains only the header, and optionally, control information. The first word of user data is located in the second burst, and the final burst may be padded to meet the 256-word length requirement. When the last burst is the short one, the packet's final burst never needs to be padded and the first word of user data may be included in the first burst.

Once the end of the packet has been indicated, the source has the option of keeping the connection open to transmit additional packets or of closing the connection.

1.1.5 Routing

The I-field contains HIPPI routing information in its 24-bit Routing Control field. This information is interpreted only by intermediate systems (switches); the Routing Control information is not interpreted when a connection is directly between two end systems.

The addresses in a Routing Control field can be in "logical addressing" or "source addressing" format. The format is indicated by the Path Selection bits of the I-field. The two formats cannot be used simultaneously in one I-field; however, both formats can be used simultaneously in one HIPPI local area network (LAN).

Note: The word *source* in "source addressing format" does not mean that the address is the source's address; it refers to the fact that the address supplied by the sending endpoint defines the complete path (route).

1.1.5.1 Logical Addressing

With logical addressing, the Routing Control field contains two 12-bit addresses: a destination (receiver's) address and a source (sender's) address, as illustrated in Figure 1-3. The order in which the addresses are placed within the field is defined by the Direction bit, as illustrated in Figure 1-3. Some switch implementations do not require inclusion of the sender's address, in which case these bits are set to zero.

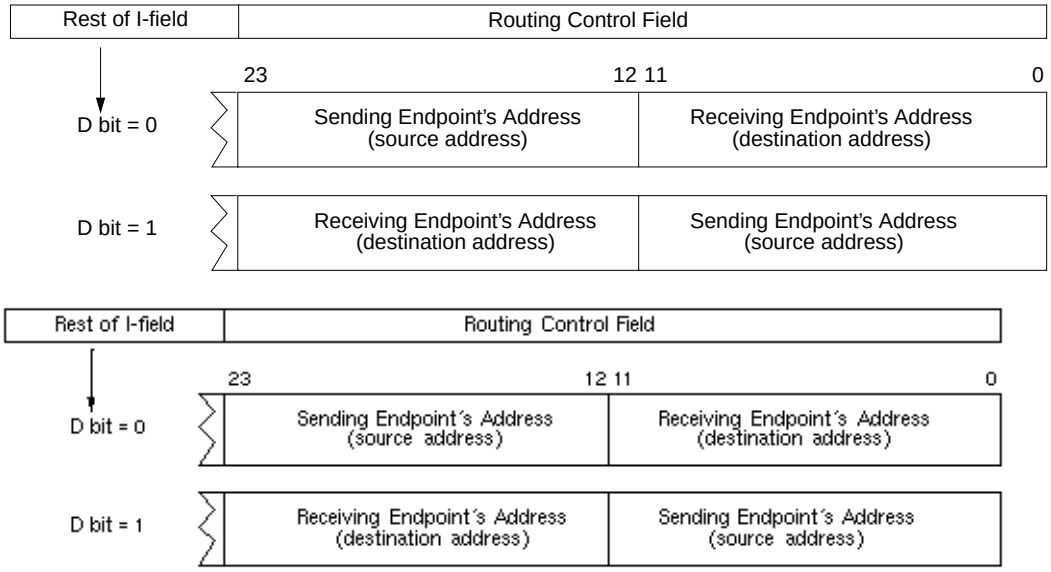


Figure 1-3 Routing Control Field with Logical Addressing

When a HIPPI LAN uses logical addressing, each HIPPI network interface (endpoint) within the LAN is assigned an address that is unique within that LAN. One address can be used for both the source and destination channels of a network interface, if desired. Assignment of these addresses is a local matter; the addresses do not need to be unique outside the particular HIPPI network. Logical addresses for LAN source and destination network interfaces have the format xxxx x0xx xxxx binary. Addresses with the format 1111 11xx xxxx binary are reserved by the HIPPI-SC standard for special assignments.

Each switch maintains a "map" of its LAN and uses a routing table to select the path along which to open a connection for each request. For example, Figure 1-4 illustrates a scenario where two paths are available between network interface A and B. When interface A requests a connection to interface B, switch 1 can select either of these paths.

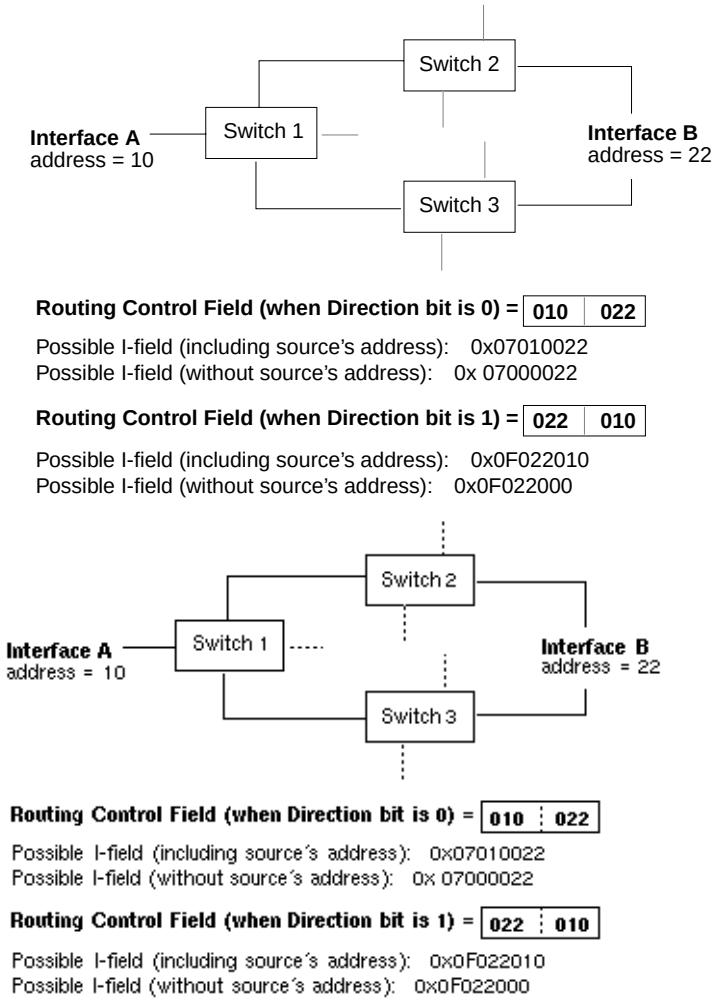


Figure 1-4 Routing with Logical Addressing

Note: All the sample I-fields (in hexadecimal notation) in Figure 1-4 include a Camp-on bit set to one.

The 12 bits make it possible to create 4096 unique endpoint addresses. The HIPPI-SC standard reserves 64 of these addresses, leaving 4032 addresses available for local assignment to HIPPI end points (for example, network interfaces).

1.1.5.2 Source Addressing

An address for source addressing can be from 1 to 24 bits long. The address is a "path" (explained in more detail below), and the Routing Control field contains one address.

When the Path Selection bits in the I-field indicate that source addressing is being used, the Routing Control field contains a list of port identifiers, as illustrated in Figure 1-5. The I-field's Direction bit determines the order in which the port identifiers are placed within the field and the alignment of (placement for) the addresses, as illustrated in Figure 1-5.

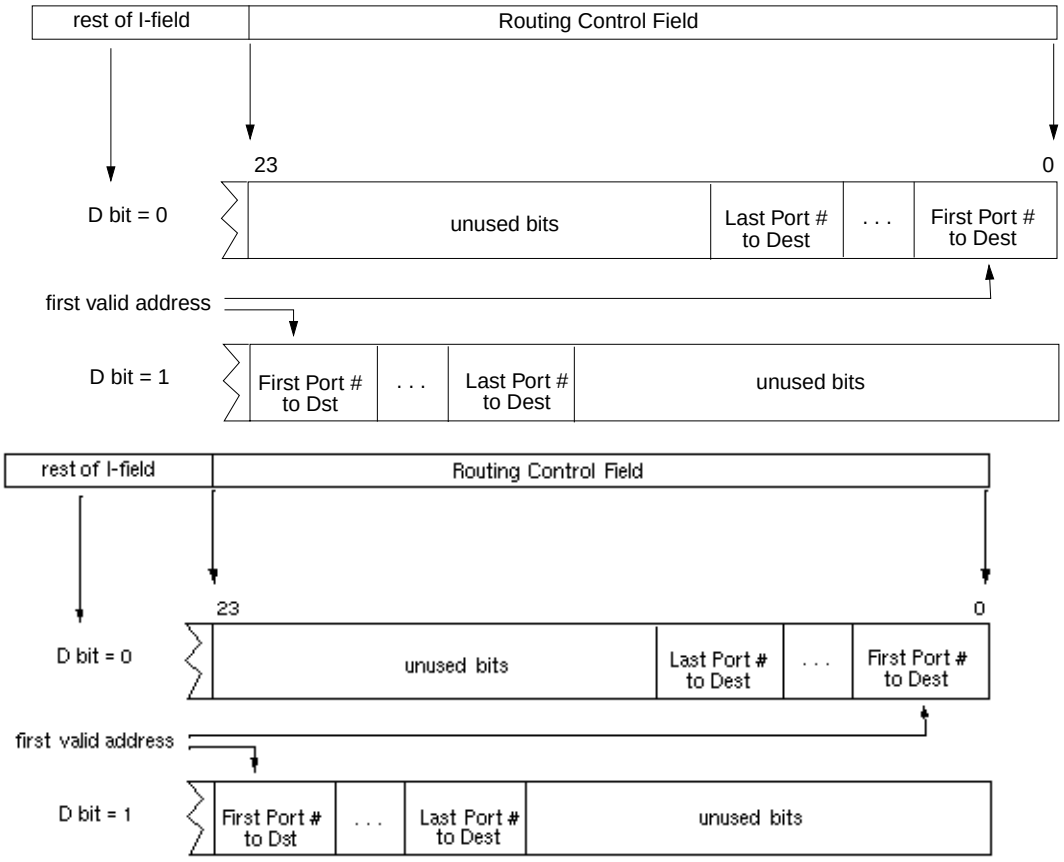


Figure 1-5 Routing Control Field (as Created by Sender) with Source Addressing

Each port identifier uniquely identifies one port within a switch. A port is a pair of physical links: both a source and a destination. For example, a 4x4 switch has 8 physical links to 4 systems, and for this it uses 4 port identifiers, as illustrated in Figure 1-6. Port identifiers are unique among all the ports on the same switch, but not among all the ports within the LAN. For example, a LAN with 5 switches might easily have 5 port identifiers of "1." Figure 1-6 is an example of the port identifiers for a LAN with 2 switches.

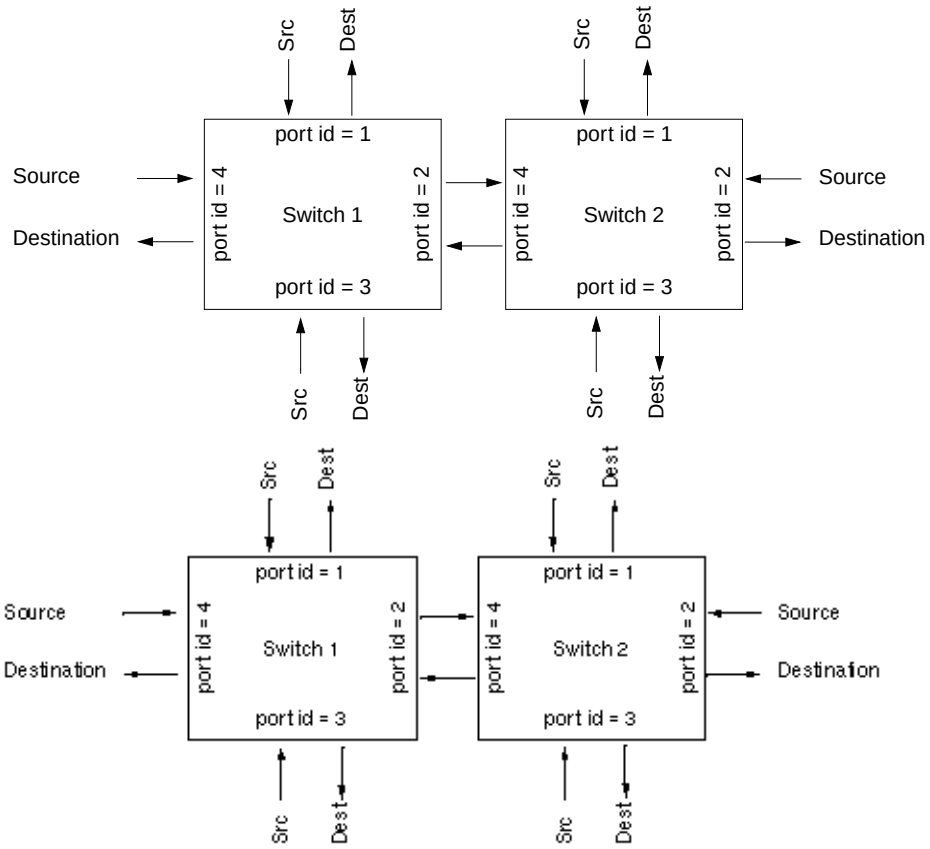


Figure 1-6 Switches with Port Identifiers

A Routing Control field in source address format is interpreted as a series of “stepping stones” in the following manner:

1. The first switch (the one attached to the source endpoint) reads the first port identifier, opens a connection at that outgoing port, and sends the I-field (that is, the connection request).
2. If the system at the end of that physical link is another switch, it reads the second port identifier, opens a connection at that outgoing port, and sends the I-field.
3. And so on, until the receiving system is the destination endpoint.

When the port identifiers are followed sequentially, they create the path between the two endpoints. Each path (address) consists of a list of all the outgoing ports through which the connection request must pass in order to reach the destination. For example, in the simplest configuration, where one switch exists between two network interfaces, the address consists of one port identifier: the one to which the receiving interface is connected, as illustrated in Example 1 in Figure 1-7. When two switches exist between the interfaces, the address consists of two port identifiers, as illustrated in Example 2 of Figure 1-7.

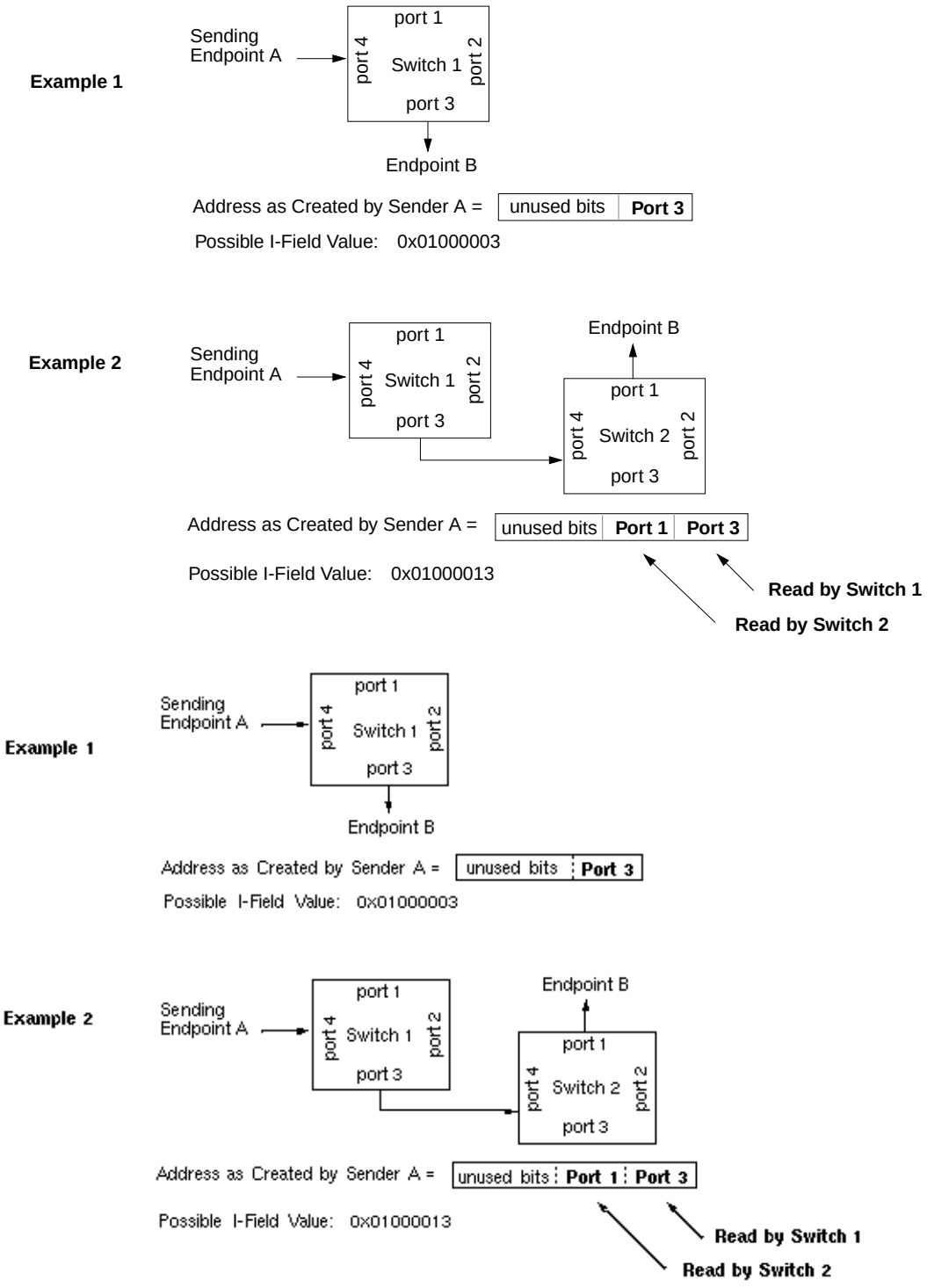


Figure 1-7 Port Identifiers for Source Addressing

Each HIPPI host within the LAN maintains a table of paths (addresses in source addressing format) for reaching each of the other endpoints. With each of its connection requests, a

source attaches one of these paths, thus indicating how to reach the destination. The path is completely defined by the sending endpoint.

The Direction bit in the I-field defines whether each port identifier should be read from the most significant or least significant end of the Routing Control field. For example, Figure 1-8 illustrates two addresses that network interface A might use to open a connection with B.

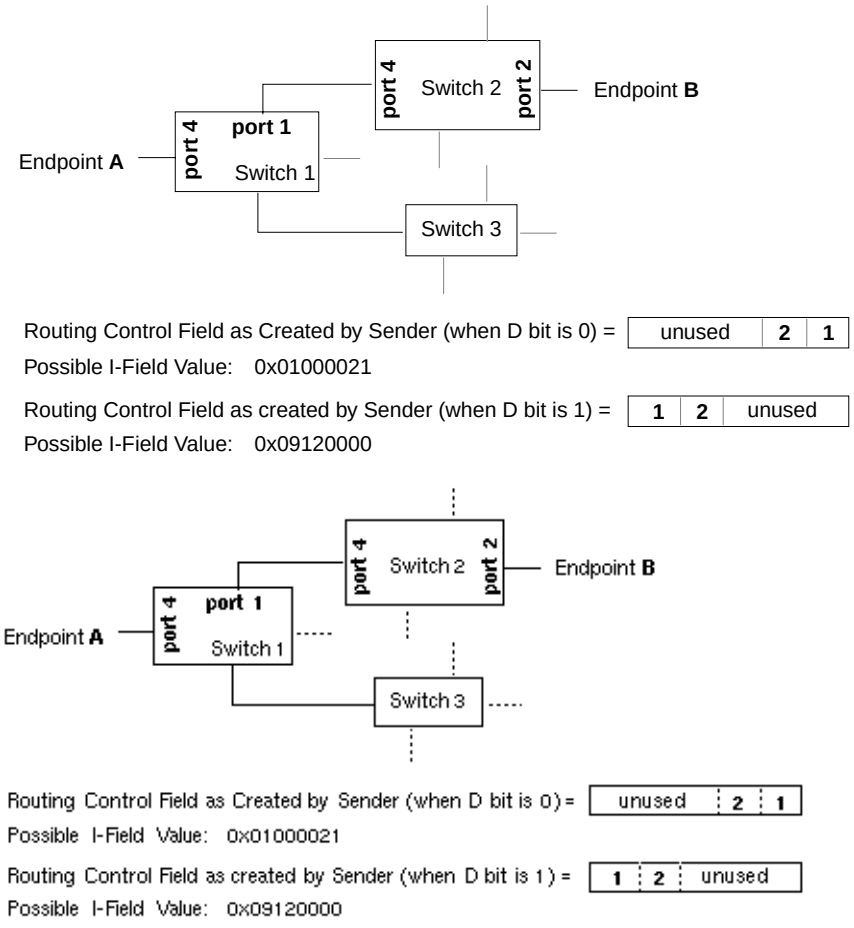


Figure 1-8 Routing with Source Addressing

Note: The sample I-Fields in Figure 1-7 and Figure 1-8 assume that the Camp-on bit is set and that the switches require four bits for each port identifier.

Unlike logical addresses (which are not altered enroute to the destination), addresses in source addressing format are changed by each switch that handles the I-field. The sender creates a list of outgoing port numbers that define a path from the sender to the receiver. By the time the packet arrives at its destination, the address has been altered so that it defines the return path (that is, the path from the receiver back to the sender). This change is brought about by each switch removing its outgoing port identifier and adding an incoming port identifier (that is, the port through which the I-field just arrived), as illustrated in Figure 1-9.

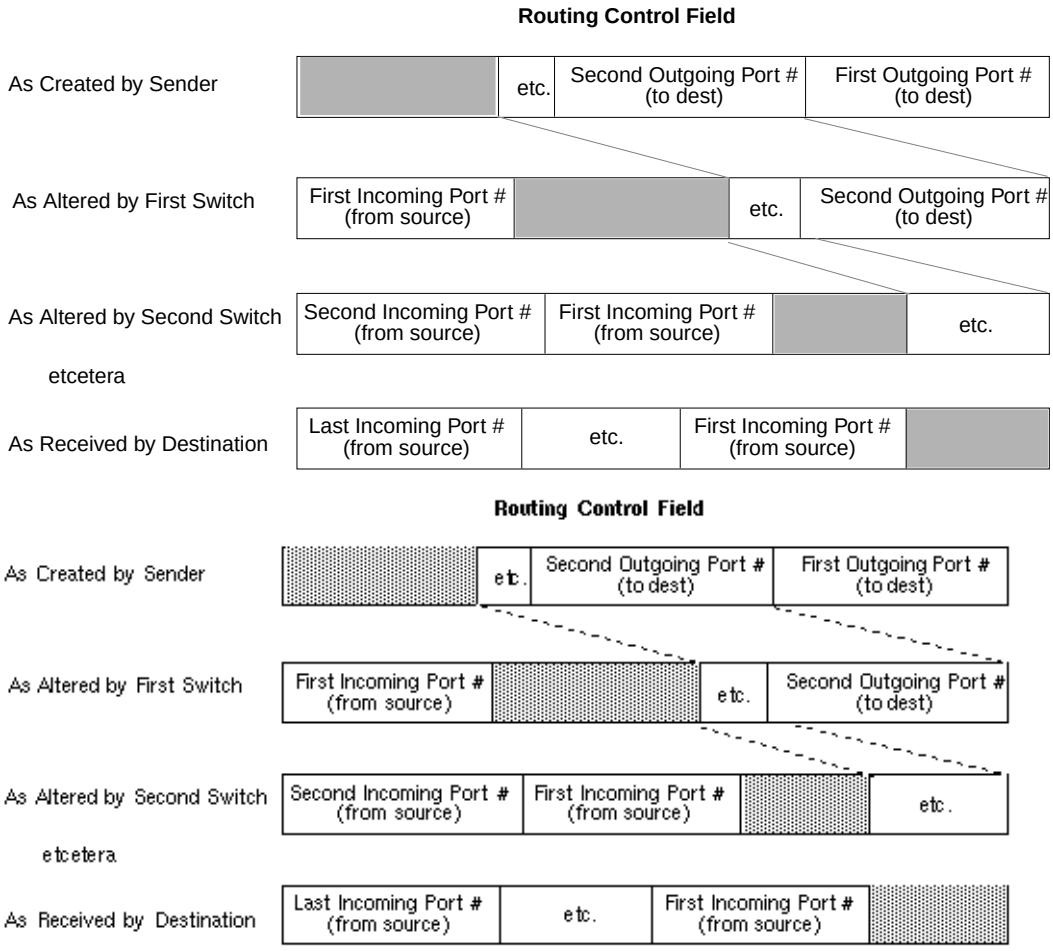


Figure 1-9 How Switches Alter Source Addresses

A destination program can copy received a Routing Control field into its own I-field and simply change the setting of the Direction bit to open a return connection, thus bypassing the table lookup procedure. Normally, the source that first creates the Routing Control field sets the D bit to zero and places the address bits in the least significant positions of the Routing Control field. The receiver changes the setting for the D bit and uses the received Routing Control field exactly as it is received. In this manner, the port identifier labeled *Last Incoming Port #* in Figure 1-9 becomes the *First Outgoing Port #* for the return connection.

Port identifiers can be one to six bits. The number of bits varies from switch to switch. The size of the port identifier is the number of bits needed to identify all the possible ports on a switch uniquely. For example, a 4x4 switch has four ports and requires at least two-bit port identifiers (binary port identifiers 00, 01, 10, and 11). If a switch is capable of being enlarged, it may use large-sized port identifiers (for example, five or six bits) to avoid a reconfiguration of all the LAN's routing tables when the switch is upgraded.

The I-field's 24-bit Routing Control field limits the number of port identifiers that can be contained in an address, as summarized in Table 1-1.

Table 1-1 Maximum Number of Port Identifiers in Routing Control Field

mber of Bits Used in Port Identifier	Maximum Number of Port Identifiers Possible in Routing Control Field
1	24
2	12
3	8
4	6
5	4
6	4

1.2 The Protocol

This section describes the format for the HIPPI I-field and FP header.

1.2.1 The I-field

The format for the 32-bit HIPPI I-field is shown in Figure 1-10, and its fields are explained in Table 1-2.

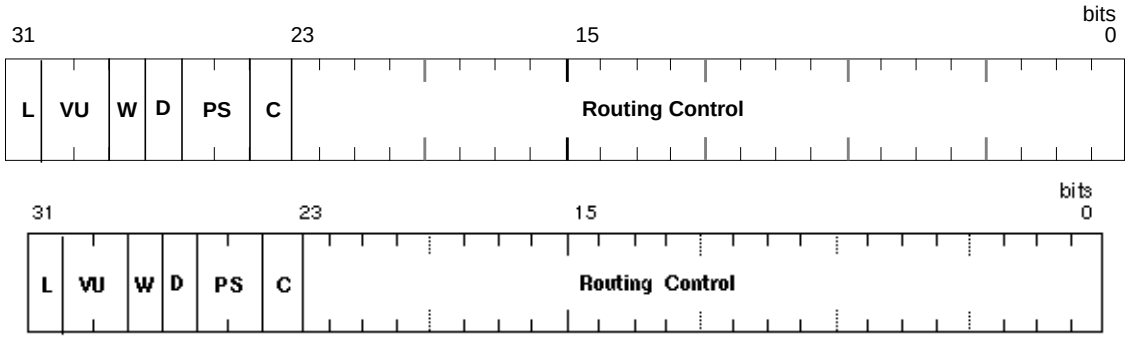


Figure 1-10 I-field Format

Table 1-2 Fields of the HIPPI I-field

Field	Bits	Description
L	31	Local or Standard Format 0 = Bits 30:0 of I-field conform to the usage described in this table. 1 = Bits 30:0 are implemented in conformance to a private (locally defined) protocol.
	30:29	Vendor Unique Bits Vendors of end-system HIPPI equipment may use these bits for any purpose. Switches do not alter or interpret these bits.
W	28	Width 0 = The data bus of the transmitting (source) HIPPI is 32-bits wide for 800 Mbits / second transmission. 1 = Source's data bus is 64-bits wide for 1600 Mbits / second transmission.
D	27	Direction 0 = Least significant bits of Routing Control field contain the destination address for the current switch to use. 1 = Most significant bits of Routing Control field contain the destination address for the current switch to use.
PS	26:25	Path Selection 00 = Source routing. 01 = Logical routing. Switch must select first route from its list of routes. 10 = Reserved. 11 = Logical routing. Switch selects any (or best) route from its list of routes.
C	24	Camp-on 0 = Switch rejects connection request immediately if port to destination is busy. 1 = Switch holds connection request if port to destination is busy and establishes connection when the port becomes free or when source aborts the request.
Routing Control	23:0	Address This field contains addressing / routing information. The contents are in source routing or logical routing format, as indicated by the PS field. For source routing, the field contains a list of switch port identifiers that, when followed, lead to the destination. For logical addressing, the field contains two 12-bit addresses (receiver's and sender's) that are used by the intermediate switches to select a route from a table.

1.2.2 The FP Header

When a HIPPI endpoint is HIPPI-FP conformant, all the packets it transmits and / or receives (without error) are HIPPI-FP packets. The first burst of each of its transmitted packets contains an FP header, and it looks for an FP header in the first burst of each received packet. A HIPPI-FP packet consists of three segments, listed below and illustrated in Figure 1-11:

- Framing Protocol Header
  This area contains the 64-bit HIPPI-FP header, described in more detail in Table 1-3.

- D1_Data
  This optional area may contain control information. The content and format are locally defined. For example, each upper-layer application (ULP-id) could use a different format for its D1 data. The D1 area can be 0 to 255 words in size.
- D2_Data
  This area contains the user / application data. This area can be 0 to (4 gigabytes minus 1 byte) in size.

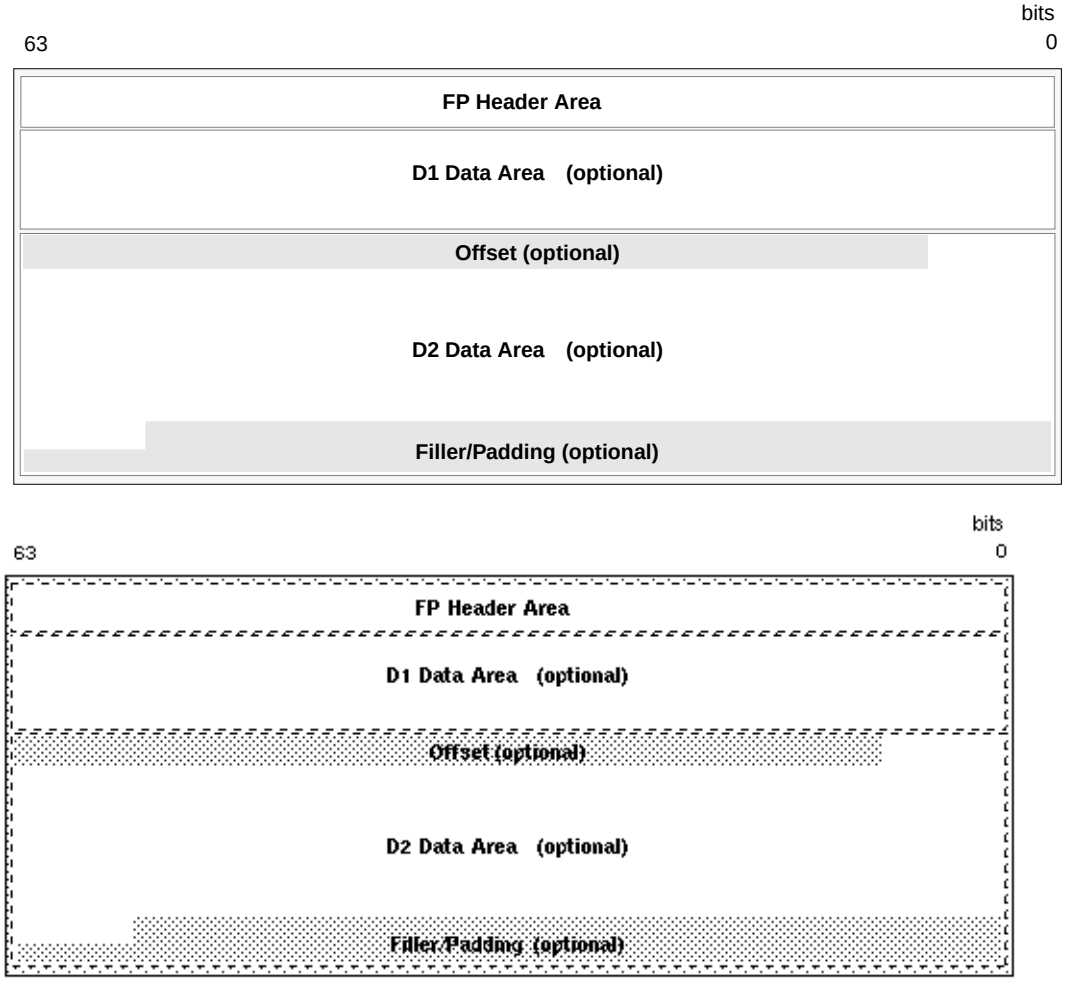


Figure 1-11 HIPPI-FP Packet Format

The 64-bit FP header describes the HIPPI packet using six fields, illustrated in Figure 1-12 and described in Table 1-3.

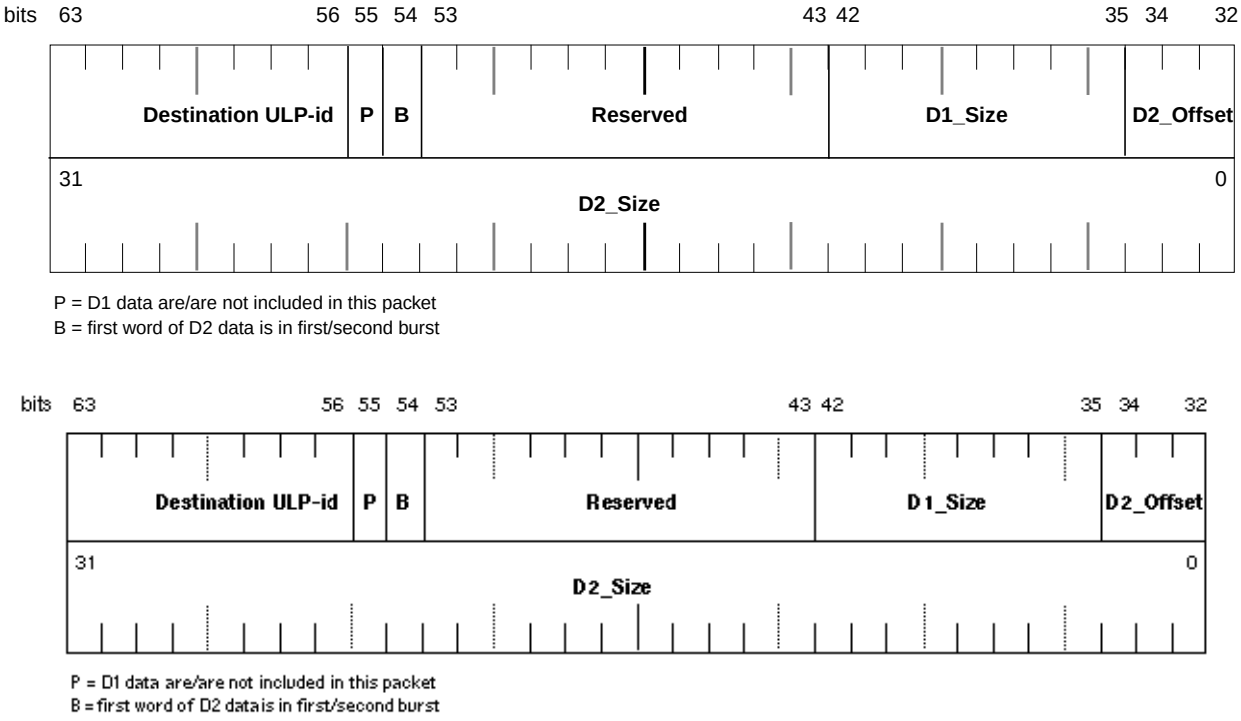


Figure 1-12 FP Header Format

Table 1-3 Fields of the HIPPI-FP Header

Field	Bits	Description
ULP-id	63:56	The 8-bit upper-layer protocol identification field identifies a system's upper-layer protocols. A transmitting application uses this number to specify the intended upper-layer recipient of the packet. A receiving HIPPI subsystem can use this number to demultiplex incoming packets among a number of upper-layer applications and to determine whether an intended recipient is known or not.
P bit	55	The 1-bit present bit indicates whether or not the packet contains D1 data.
B bit	54	The 1-bit burst boundary bit indicates which burst contains the first byte of D2 data. D2 data can be included in the first burst or can start with the first word of the second burst.
D1 Size	42:35	The 8-bit D1 size field indicates the number of 64-bit words of D1 data included in this packet.
D2 Offset	34:32	The 3-bit D2 offset field indicates the number of bytes between the last byte of D1 data and the first byte of D2 data.

Table 1-3 Fields of the HIPPI-FP Header

Field	Bits	Description
D2 Size	31:0	The 32-bit D2 size field indicates the number of bytes of D2 data included in this packet. Bytes of offset or fill are not included in this count.

1.3 HIPPI Network Configurations

This section describes some of the common configurations of HIPPI equipment. Because HIPPI is a simplex point-to-point protocol, only one network interface at a time can transmit onto the transport medium (cable) between two endpoints. Two physical links (cables) are required for bidirectional communication. This aspect of HIPPI makes it quite different from protocols such as Ethernet, FDDI, or 802.5 Token Ring.

1.3.1 Basic HIPPI Configurations

A basic (non-networked) HIPPI configuration consists of two endpoints, with one sending and the other receiving, as shown in Figure 1-13. To exchange data in both directions, two physical links and two connections are required between the two endpoints, as shown in Figure 1-14. Each endpoint's source channel must open a connection with the destination of the other endpoint.

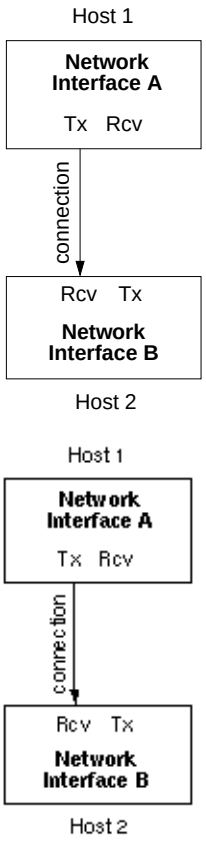


Figure 1-13 Basic HIPPI Configuration

The IRIS HIPPI network interface board has two channels (I/O ports). It treats each one as a separate entity, so each IRIS HIPPI network interface supports two autonomous, simultaneous connections: one sending data and one receiving data. The two channels can be communicating with two different endpoints (as shown by the examples on the right in Figure 1-14) or to the same endpoint (as illustrated by the example on the left in Figure 1-14). TCP/IP over HIPPI requires the latter configuration.

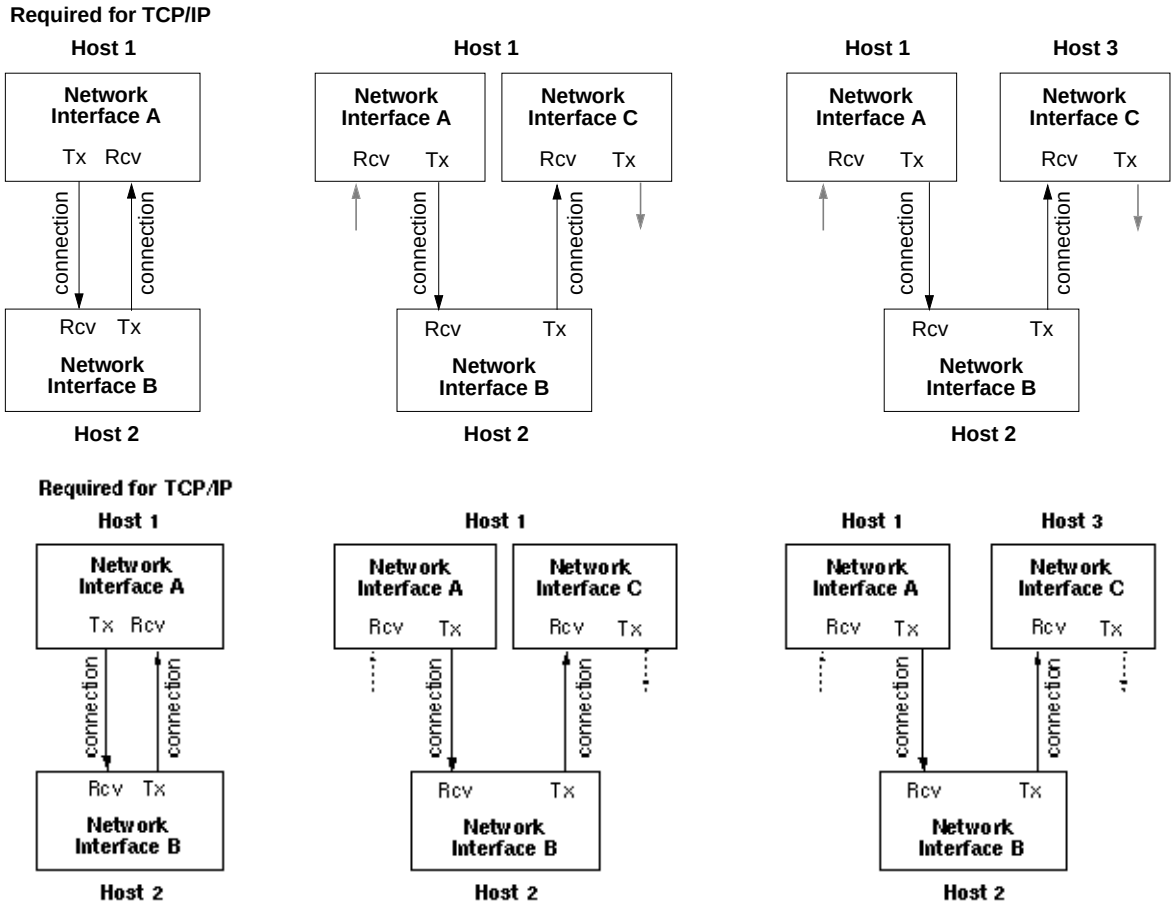


Figure 1-14 Variations of the Basic HIPPI Configuration

1.3.2 HIPPI Local Area Network Configurations

A switch may be placed along the point-to-point physical link (between two HIPPI endpoints), making it possible to configure a number of endpoints into a HIPPI local area network (LAN, or fabric). Configuring the endpoints in this way does not alter the fact that each communication is a point-to-point connection. Before a packet can be sent, a dedicated connection must be opened along the entire path between the sending (source) endpoint and the receiving (destination) endpoint, and each HIPPI link can support only one connection at a time.

When a switch is included in a HIPPI configuration, each endpoint has a number of hosts with which it can communicate (one at a time). Figure 1-15 illustrates a HIPPI LAN with one switch. The switch in this illustration is a 4 x 4, meaning that the switch can have four systems (8 HIPPI cables) attached to it. The switch supports four simultaneous connections. For example, in Figure 1-15, any one of the following connection scenarios could be occurring at a single point in time:

- A and D could be exchanging TCP/IP traffic. There would be two connections open between them. C and B could be doing the same. This scenario opens all four possible connections.
- A could be transmitting to B, while B transmitted to C, C to D, and D to A. This scenario also opens four connections.
- A and C could be exchanging bidirectional traffic. D could be transmitting to B. Only three connections are open in this scenario.

Figure 1-16 illustrates a LAN with multiple switches, and Figure 1-17 illustrates a complex HIPPI LAN including a long distance fiber optic link and multiple ports between switches to improve connection setup time by reducing the probability of encountering a busy link.

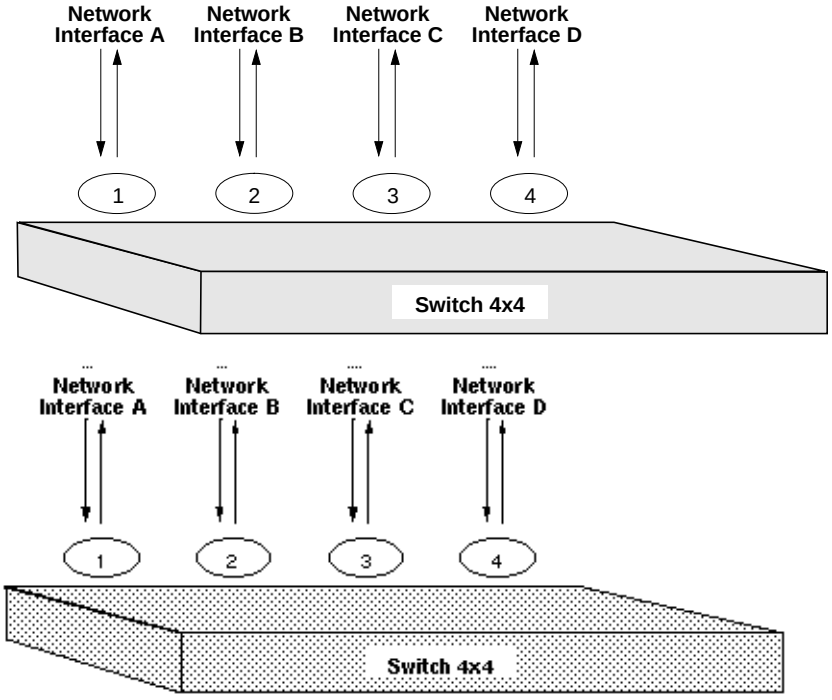
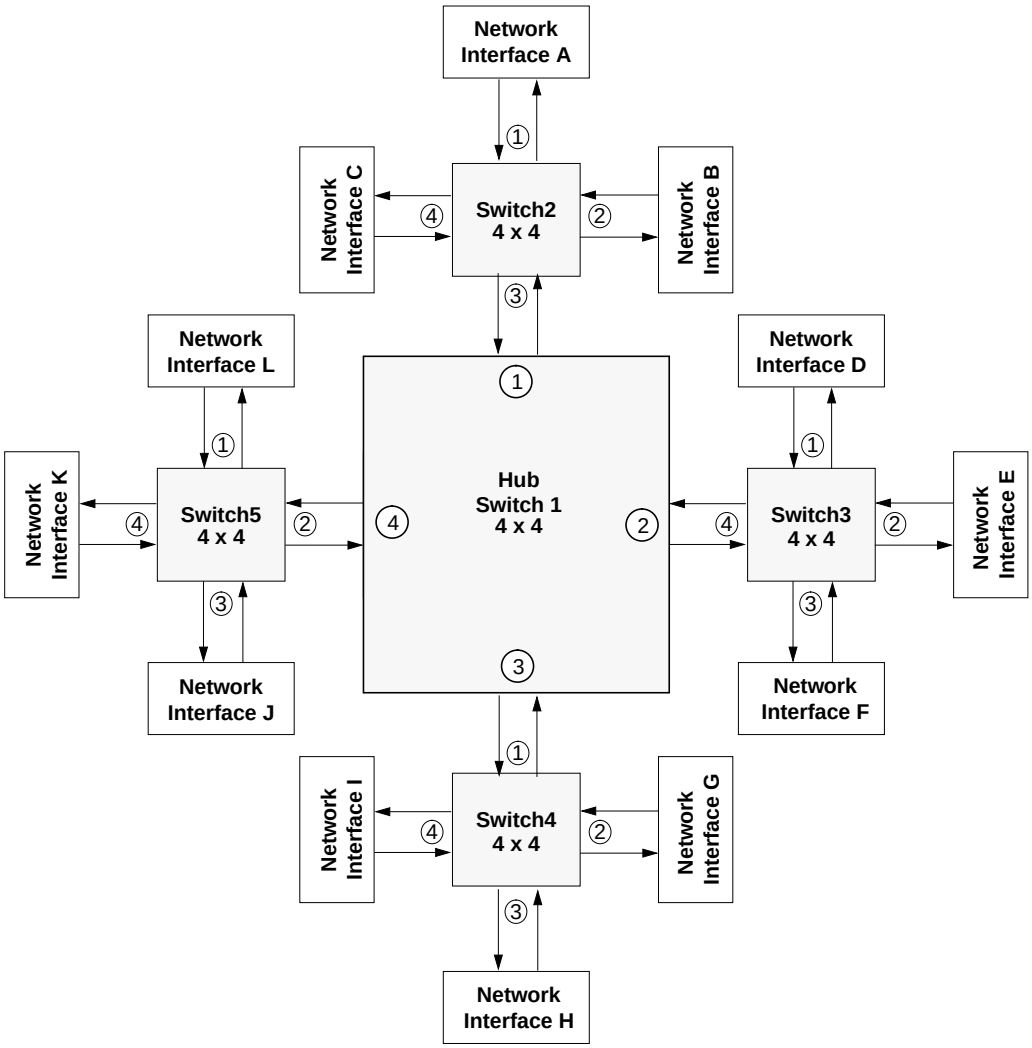


Figure 1-15 HIPPI LAN Configuration with One Switch


Network Interface A
Network Interface C
Switch2 4 x 4
Network Interface B
Network Interface L
Network Interface D
Network Interface K
Switch5 4 x 4
Hub Switch 1 4 x 4
Switch3 4 x 4
Network Interface E
Network Interface J
Network Interface F
Network Interface I
Switch4 4 x 4
Network Interface G
Network Interface H

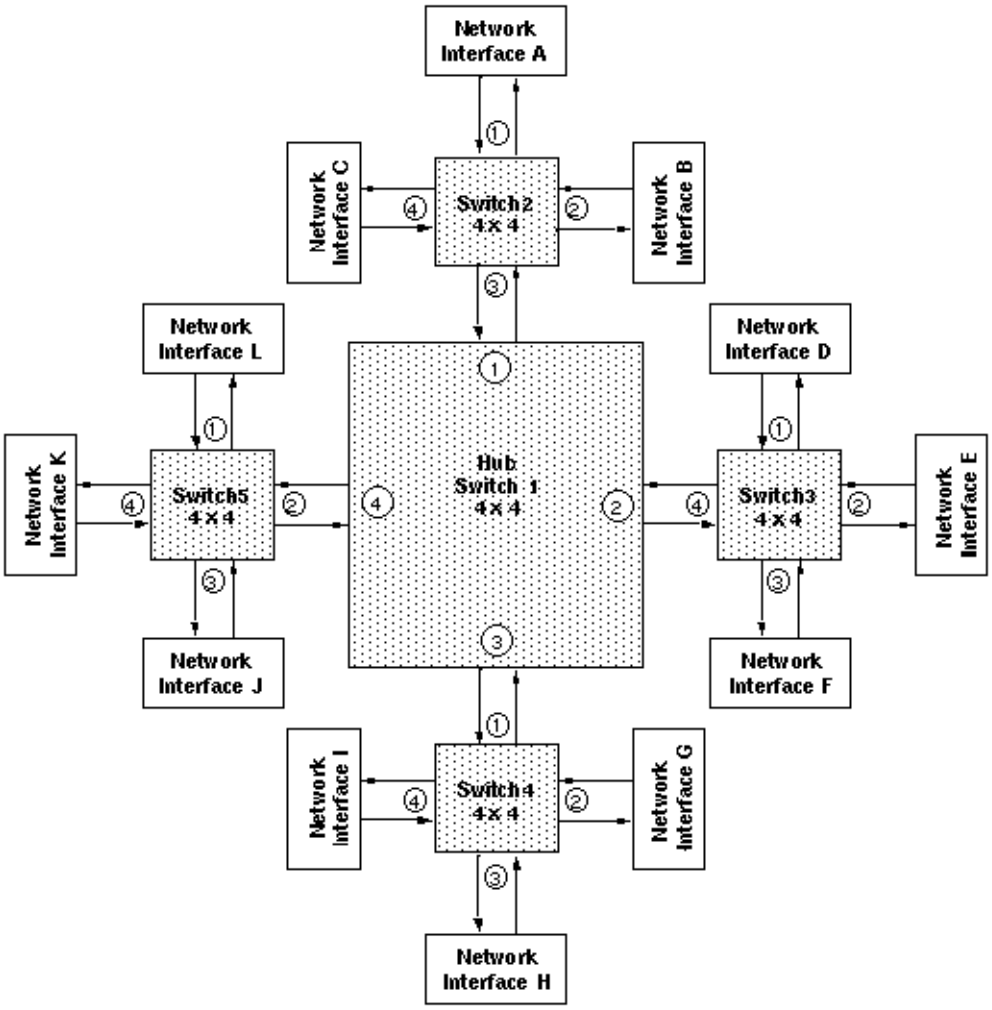
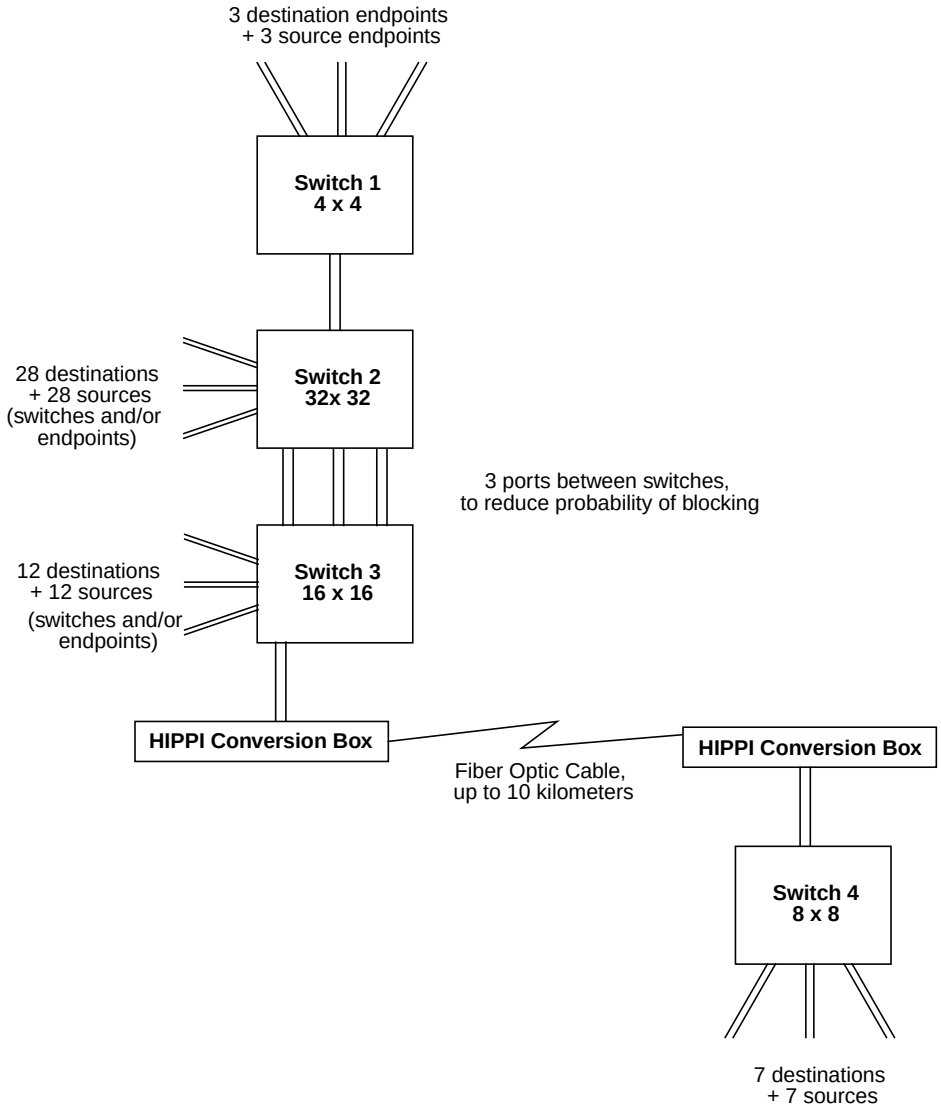


Figure 1-16 HIPPI LAN Configurations with Multiple Switches


3 destination endpoints
+ 3 source endpoints
Switch 1
4 x 4
28 destinations
+ 28 sources
(switches and/or
endpoints)
Switch 2
32x 32
3 ports between switches,
to reduce probability of blocking
12 destinations
+ 12 sources
(switches and/or
endpoints)
Switch 3
16 x 16
HIPPI Conversion Box
Fiber Optic Cable,
up to 10 kilometers
HIPPI Conversion Box
Switch 4
8 x 8
7 destinations
+ 7 sources

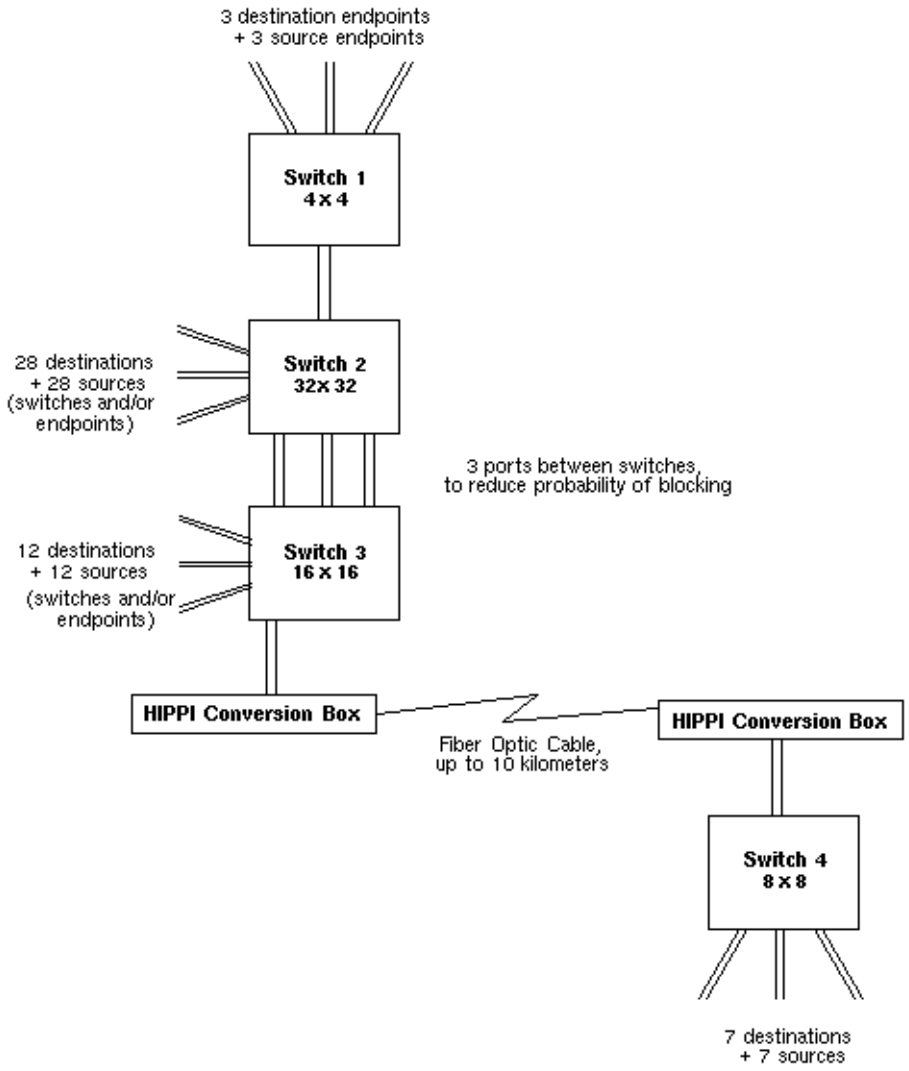


Figure 1-17 Complex HIPPI LAN Configuration

The maximum number of switches and endpoints within a LAN is limited by three factors:

- When logical routing is used, the 12-bit HIPPI address (half of the Routing Control field) limits the number of unique endpoint addresses to 4096. It is possible for a site to implement this number of networked HIPPI endpoints; however, to be compliant with the HIPPI-SC standard, 64 reserved addresses should not be assigned to local endpoints / hosts. This limits the number of endpoints to 4032 per LAN. There is no limit to the number of switches when logical routing is used.
- When source routing is used, the I-field's 24-bit Routing Control field limits the number of port identifiers that can be included in the list. The exact number depends on the sizes of the port identifiers used by the switches along the specific endpoint-to-endpoint path, as explained in Section 1.1.5. Each port identifier in the Routing Control field represents one switch along the path. Table 1-4 summarizes the maximum number of switches along any point-to-point path within a HIPPI LAN,

assuming that all switches along that path use port identifiers of the same size. (This assumption does not reflect actual site configuration practices, but is useful here for illustration of a point.) When source routing is used, the number of switches and endpoints that are possible is not limited, but the number of switches between any two endpoints within the LAN is limited.

Table 1-4 Maximum Number of Switches Along Any Single Point-to-point Path When Using Source Addressing

Number of Bits Used For All Port IDs in Routing Control Field	Max. Number of Switches Along Any Single Point-to-point Path
1	24
2	12
3	8
4	6
5	4
6	4

- If a LAN is built according to the guidelines in Appendix B of RFC 1374, the recommended maximum number of hops (switches) between any two endpoints is three. This limit has major implications for the structure and size of a HIPPI LAN. The structure is limited to a single hub switch with satellite switches attached to the hub's ports, but no switches attached to any satellite ports. Figure 1-16 shows an example of a LAN designed in accordance with the RFC 1374 guidelines. Table 1-5 summarizes the maximum number of switches and endpoints possible for a LAN in which switches of only one size are used throughout the LAN.

Table 1-5 Maximum Number of Switches and Endpoints on a LAN Built in Accordance with RFC 1374, Appendix B Guidelines

4 x 4	8x 8	16 x 16	32 x 32	64 x 64
5 switches / 12 endpoints	9 switches / 56 endpoints	17 switches / 240 endpoints	33 switches / 992 endpoints	65 switches / 4032 endpoints

1.4 HIPPI Standards and Documentation

- ANSI HIPPI-PH
  The *HIPPI Mechanical, Electrical, and Signalling* (HIPPI-PH) standard defines the physical layer: electrical and mechanical aspects of HIPPI cables, as well as the behavior of HIPPI physical interfaces (including the HIPPI signals, like **REQUEST**, **CONNECT, READY**, and **PACKET**).
- ANSI HIPPI-SC
  The *HIPPI Physical Switch Control* (HIPPI-SC) standard defines switch behavior, routing methods, and connection management. The HIPPI I-field is defined by this standard.

- ANSI HIPPI-FP
  The *HIPPI Framing Protocol* (HIPPI-FP) defines data-framing issues: how a packet is formed, how its data contents are described and interpreted. The HIPPI-FP packet (FP header, D1_Data, and D2_Data) is defined by this standard.
- ANSI HIPPI-LE
  The *HIPPI Encapsulation of ISO 8802-2 (IEEE 802.2) Logical Link Control Protocol Data Units* (HIPPI-LE) standard defines the method for encapsulating (and thus interoperating with) 802.2-compliant data link layers such as FDDI, 802.5 Token Ring, and CSMA / CD (Ethernet).
- ANSI HIPPI-IPI-3 for Disk
  The *HIPPI Intelligent Peripheral Interface — Device Generic Command Set for Magnetic and Optical Disk Drives* standard defines an upper-layer protocol for interfacing disks to the HIPPI subsystem.
- ANSI HIPPI-IPI-3 for Tape
  The *HIPPI Intelligent Peripheral Interface — Device Generic Command Set for Magnetic Tape Drives* standard defines an upper-layer protocol for interfacing tapes to the HIPPI subsystem.
- RFC 1374
  IP and ARP on HIPPI, by J. Renwick and A. Nicholson (October 1992) recommends a standards track protocol for using the IP suite of network and transport layer protocols over HIPPI.

The ANSI documentation for HIPPI standards is maintained by the American National Standard of Accredited Standards Committee (ANSI X3T9.3). Copies of the ANSI standards listed above can be obtained by writing or calling the following:

Don Tolmie, Chairperson
Los Alamos National Laboratory
C-5, MS-B255
Los Alamos, NM 87545
Telephone: 505-667-5502
Internet email: det@lanl.gov

1.5 Theory of Operations for IRIS HIPPI

This section provides a brief description of the IRIS HIPPI hardware.

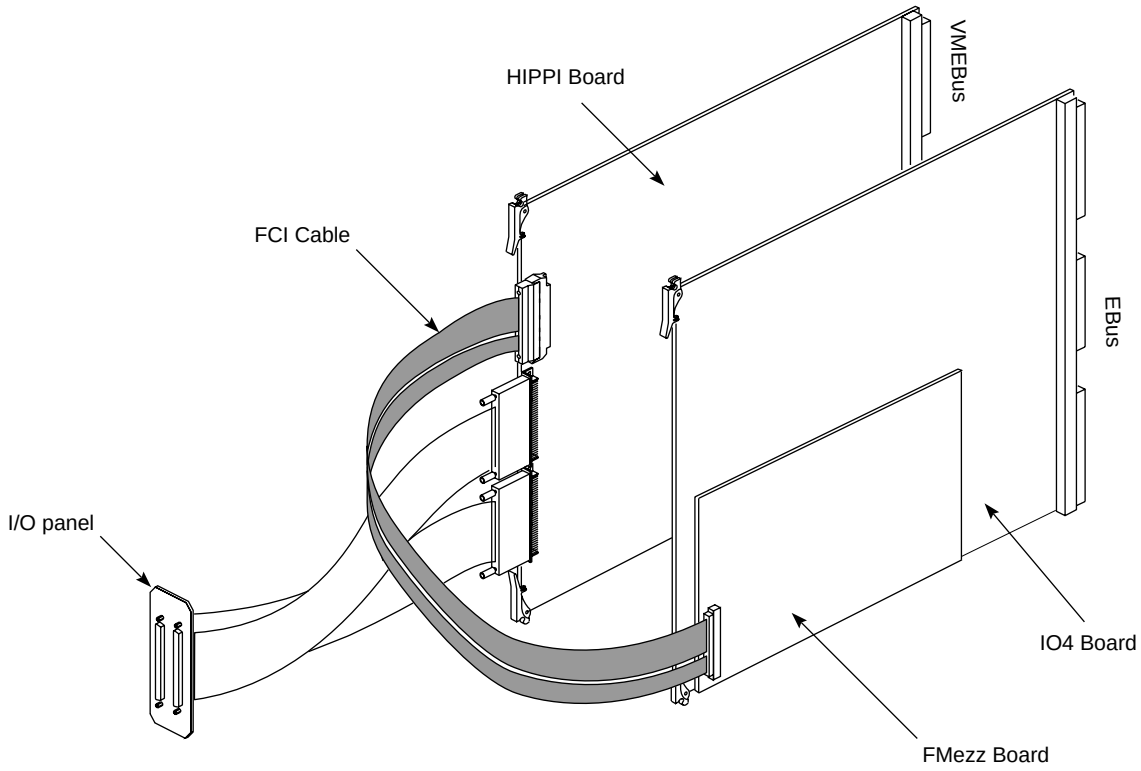
The IRIS HIPPI product consists mainly of the following hardware components:

- FCI mezzanine (FMezz) board
- FCI cable
- HIPPI Board

Of the hardware components, only the HIPPI board contains logic specific to the HIPPI protocol. The HIPPI board communicates with another HIPPI node (device) through the HIPPI connectors on the CHALLENGE or Onyx system's I / O panel. The HIPPI board communicates with the CHALLENGE or Onyx systems's operating system through the

IBus, using a Flat Cable Interface (FCI) between the HIPPI board and the mezzanine (FMezz) board. The mezzanine board, installed onto any IO4 board, provides access to the IBus. Figure 1-18 illustrates how the HIPPI hardware looks when all the parts are connected together. (The relationships and positioning is different for each configuration, but the overall connections are the same for all installations.)

figs/overview.ai 100%



This illustration accurately displays the connections between components. The positioning shown does not reflect actual positions when the components are installed.

Figure 1-18 General Overview of IRIS HIPPI Hardware

1.5.1 The FCI Mezzanine Board

The FCI mezzanine (FMezz) board shipped with the IRIS HIPPI package occupies one short mezzanine slot on any IO4 board. It is not necessary to use this shipped board; the HIPPI board can be attached to any standard FMezz board (long or short). A long FMezz board provides connections for I/O adapters 2 and 5 (lower mezzanine position), or 3 and 6 (upper position) on the IO4 board's IBus; the short mezzanine board provides connections for I/O adapters 5 or 6. (See the "Theory of Operations" chapters in the *CHALLENGE/Onyx Deskside Installation Instructions* or *CHALLENGE/Onyx XL Rackmount Installation Instructions* for further details on the IBus, IO4 boards, and I/O adapters.)

1.5.2 The FCI Cable

The FCI (flat cable interface) cable connects the HIPPI board to the FCI mezzanine (FMezz) card, thus providing the data path between the HIPPI board and the IBus.

1.5.3 The HIPPI Board

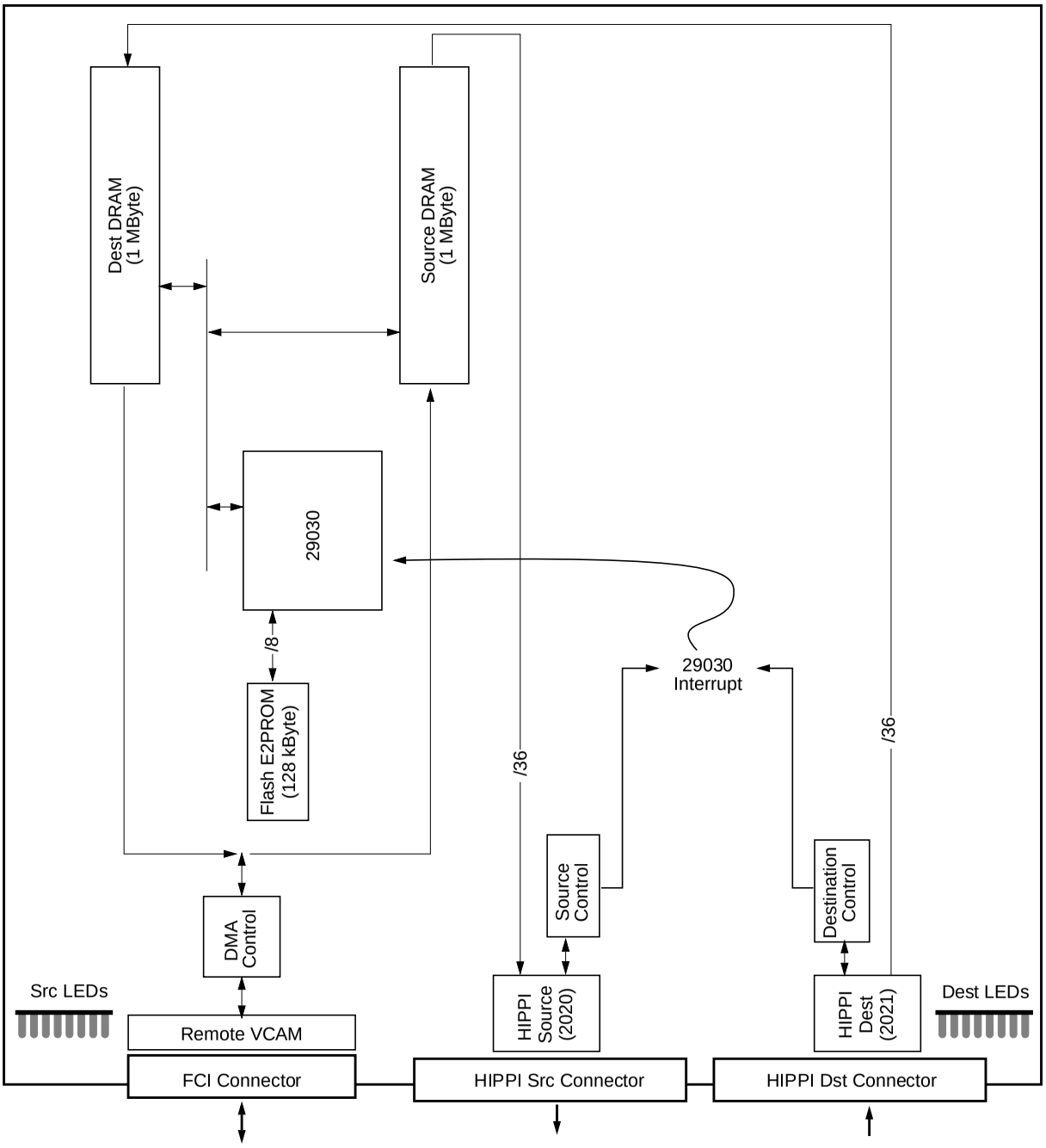
The HIPPI board is a 9U VME form factor printed circuit board supporting two HIPPI channels (receive and transmit) that exchange data with ANSI HIPPI-compliant stations and switches. It occupies one VMEBus slot, where it obtains power. The HIPPI board does not use the VMEBus protocol or data path; it uses the FCI cable (connecting to the IBus) for all communication with the local host system. The HIPPI board contains logic that allows it to function as an I/O adapter on any IO4 board's IBus. HIPPI data traverses the following path: HIPPI I/O port, internal HIPPI cable, HIPPI board, FCI cable, FMezz card, IBus on IO4 board, Ebus, host memory.

Because it resides in a VMEBus slot, the HIPPI board has many features of a standard VMEBus board; however, because it is not a VMEBus device, it is also different in many respects. The most important similarities and differences are listed below:

- Similarities
  - The HIPPI board has VMEBus P1, P2, P3 connectors.
  - When installed, it jumpers its VMEBus slot, thus making the bus signals available to VMEBus boards that are installed downstream from it.
  - Its VMEBus slot must be serviced by the card cage's power modules.
- Differences
  - The HIPPI board's throughput is not restricted to VMEBus data rates.
  - The HIPPI board does not require the services of a VCAM board.
  - It does not use the VMEBus protocol, so does not need to be configured for VMEBus parameters such as interrupt level, bus grant/request priority levels, and VME address.

The IRIS HIPPI board typically uses 75 watts of power, drawn from its VMEBus slot. The board requires 5 volts at a maximum of 15 amps and 12 volts at a maximum of 1.5 amps.

Figure 1-19 is a block diagram of the HIPPI board, showing the main data paths for the board. The board has separate banks of on-board memory (triple-port DRAM) for buffering data between the host and each autonomous HIPPI channel. The board also has a Flash E^2PROM that holds the HIPPI firmware and the board's diagnostics; the firmware can be rewritten (upgraded) by the driver if it is found to be out of date when the driver is initialized.


Dest DRAM (1 MByte)
Source DRAM (1 MByte)
29030
/8
Flash E2PROM (128 kByte)
29030 Interrupt
/36
/36
Source Control
Destination Control
DMA Control
Src LEDs
Dest LEDs
HIPPI Source (2020)
HIPPI Dest (2021)
Remote VCAM
FCI Connector
HIPPI Src Connector
HIPPI Dst Connector

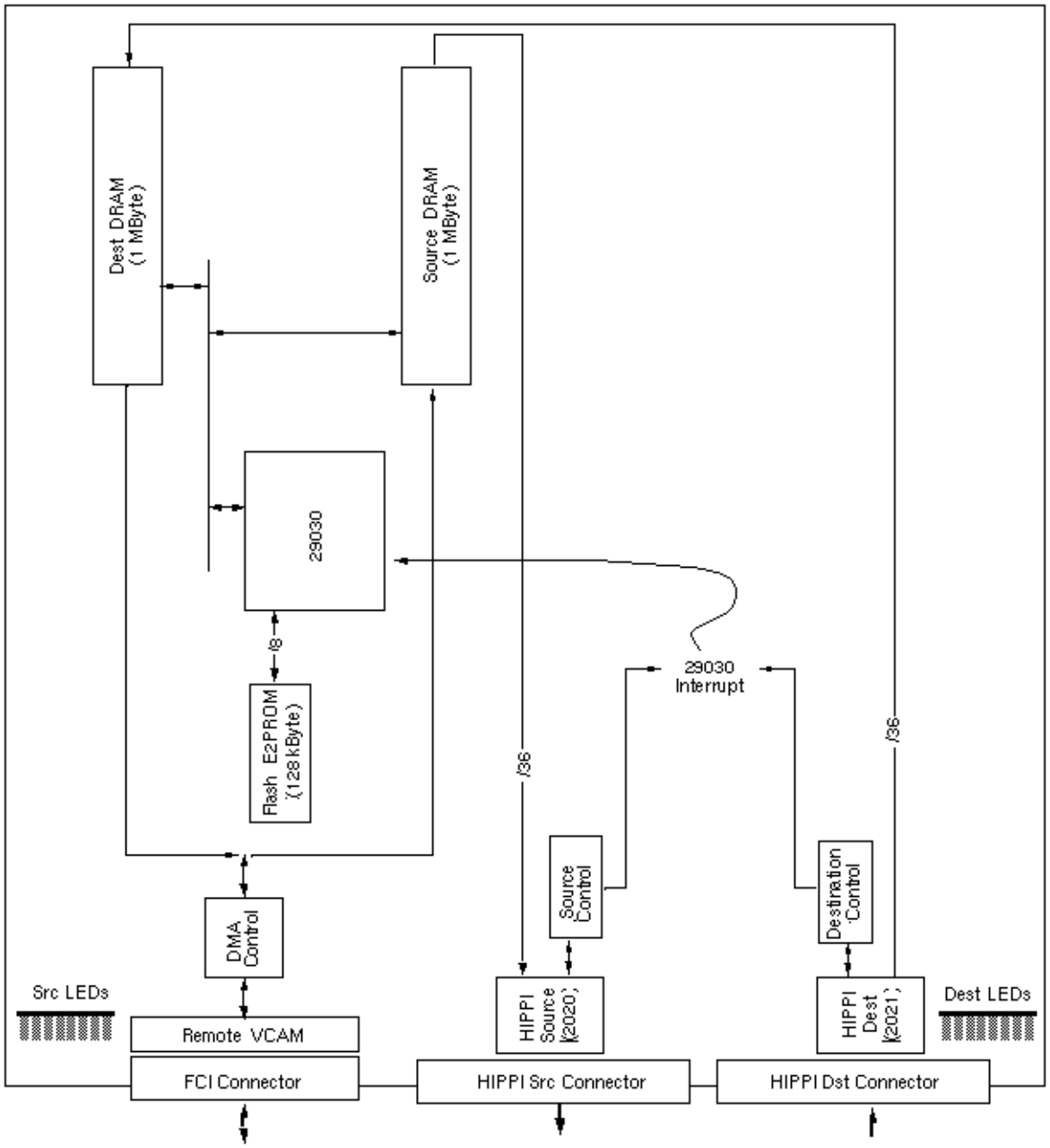


Figure 1-19 Block Diagram of HIPPI Board

Chapter 2

Installing the HIPPI Board

This chapter describes how to install the IRIS HIPPI network interface controller hardware into a CHALLENGE™ or Onyx™ server or supercomputer. There is a separate section for each of the following platforms:

- CHALLENGE L Deskside
- CHALLENGE XL Rackmount
- Onyx Deskside
- Onyx Rackmount

Warning: **Installing this equipment requires specific training and technical knowledge. These instructions are provided for use only by Silicon Graphics system support engineers (SSEs) or other personnel trained by Silicon Graphics. This equipment uses internal electrical power that is hazardous if the equipment is improperly handled.**

2.1 Installation for CHALLENGE L Deskside System

This section describes the steps for installing the IRIS HIPPI network product into a CHALLENGE L Deskside server. The CHALLENGE L Deskside platform supports up to four IRIS HIPPI boards.

Warning: **Installing this equipment requires specific training and technical knowledge. These instructions are provided for use only by Silicon Graphics system support engineers (SSEs) or other personnel trained by Silicon Graphics. This equipment uses internal electrical power that is hazardous if the equipment is improperly handled.**

2.1.1 Preparing for Installation

Before starting the installation, prepare yourself and the equipment by following the instructions below.

2.1.1.1 Check the IRIS HIPPI Package for Completeness

Verify that the IRIS HIPPI package is complete. It should contain the items listed in Table 2-1.

Table 2-1 IRIS HIPPI Package Contents

Item	Quantity
Short FCI mezzanine board	1
HIPPI board	1
Teflon-covered FCI (flat cable interface) cable assembly	1
Internal HIPPI cable assembly (includes 2 cables, 4 standoffs, and panel plate)	1
Screws for attaching mezzanine board	4
Labels with adapter IDs	3 sheets
CD-ROM with software (including online release notes)	1
Documentation: *IRIS HIPPI API Programmer's Guide* and *IRIS HIPPI Administrator's Guide*	2 manuals

If anything is missing, do not proceed with the installation. Contact the customer or the customer's salesperson.

2.1.1.2 Prepare the CHALLENGE System

Follow the instructions in this section to prepare the CHALLENGE L Deskside system for installation.

Caution: This equipment is extremely sensitive and susceptible to damage by electrostatic discharge (ESD), a spark caused by the buildup of electrical static potential on clothing and other material. You must use proper ESD preventive measures as explained in the "Safety" section of the *CHALLENGE/Onyx Deskside Installation Instructions*.

1. Verify that the IRIX operating system is the correct version for this IRIS HIPPI release using the command below. Do not proceed until the correct version of IRIX is installed, as described in the *IRIS HIPPI Release Notes*.

   ```
   % versions eoe1
   I  eoe1  date  Execution Only Environment 1, version
   ```

2. Verify that the file system is backed up.

3. Optional, but recommended, step.
   Install the IRIS HIPPI software, and do the required configuration steps. Step-by-step instructions are provided in the *IRIS HIPPI Release Notes* and the *IRIS HIPPI Administrator's Guide*. When the software is installed and configured, continue with the next step in these instructions.

Note: You cannot verify successful installation of the board until the software is installed. If you choose not to install the software now, you will need to do so after the board has been installed.

4. Shut down the system by turning the key on the System Controller panel (located at the front) to **OFF**. Wait a minute for the system to shut down, then switch the circuit breaker on the back to **OFF**.

Warning: **Failure to turn off the circuit breaker may result in electrical shock. Failure to wait for the system to shut down may cause irreparable damage to system components or data.**

5. Open the front door and pull down the I/O panel in the front of the chassis to expose the VMEBus slots and IO4 boards.

2.1.2 Selecting Mezzanine and VME Slots

To install the IRIS HIPPI network hardware, you need to locate two available slots in the CHALLENGE chassis: one mezzanine slot (position) and one VMEBus slot. Table 2-2 lists the slots from which you can select. It is recommended that the mezzanine and VMEBus slots be as close to each other as possible because the FCI cable will connect them. However, the FCI cable is long enough to accommodate any boards in a properly configured CHALLENGE Deskside system.

Table 2-2 Slots for IRIS HIPPI Installation in CHALLENGE Deskside System

Slots Required	Slots That Can Be Used
Short mezzanine slot	Upper or lower mezzanine slot on an IO4 board in slot 5, 4, or 3
VMEBus slot	Slot 7, 8, 9, 10, or 11

Note: Instead of installing the FMezz board shipped with the IRIS HIPPI product, you may select an FCI connection on an already installed FMezz board (long or short). If you take this option, some of the steps in the section on installing the FMezz board can be skipped; however, other steps are relevant and very important, so do not skip the section.

2.1.2.1 Select a VMEBus Slot

The VMEBus slots of the CHALLENGE Deskside backplane that can be used for IRIS HIPPI are listed in Table 2-2 and illustrated in Figure 2-1. Select the first unoccupied slot for the HIPPI board. Slot 7 is the first VMEBus slot; slot 8 is the second; and so on.

Note: If you select a slot that is not the first available slot (that is, if you skip a VMEBus slot), follow the instructions in the *CHALLENGE/Onyx Deskside Installation Instructions* for jumpering across skipped slots.

The IRIS HIPPI board typically uses 75 watts of power, drawn from its VMEBus slot. The board requires 5 volts at 15 amps and 12 volts at 1.5 amps. Verify that the slot you have chosen has appropriate power modules installed, that total system power consumption

remains within the available power aupplied, and that heat dissipation / ventilation for this card cage can handle this additional board.

Because the IRIS HIPPI board occupies and jumpers a VMEBus slot (just like a normal VMEBus board), regular VMEBus boards may be installed in the slots downstream from the HIPPI board.

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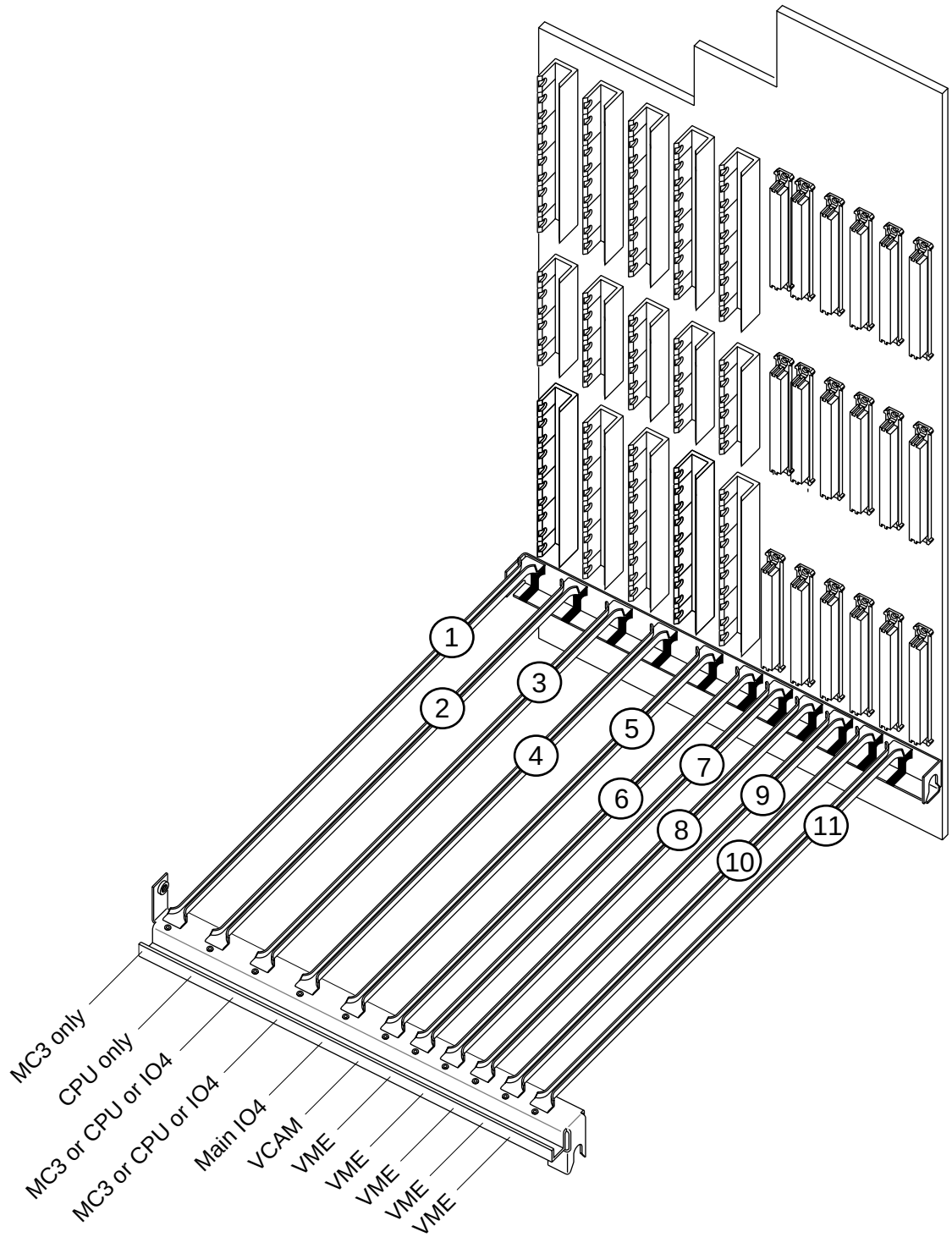

Figure 2-1 CHALLENGE Deskside IO4 and VMEBus Slots

2.1.2.2 Select a Mezzanine Slot

Locate the IO4 boards that are currently installed. As illustrated in Figure 2-1, slot 5 always has an IO4 board and slots 4 and 3 may contain IO4 boards. (A CHALLENGE L may have one to three IO4 boards installed.) Two mezzanine slots are located on each IO4 board. The short FCI mezzanine board included in the IRIS HIPPI package may be installed on any of the available mezzanine slots.

Note: When installing an additional IRIS HIPPI network connection, be aware that the ordering of the FMezz boards determines the assignment of IP network interfaces to the IRIS HIPPI boards. During startup, the first FMezz board that is found with a HIPPI board attached is assigned network interface *hip0*; the second is assigned *hip1*, and so on. See Chapter 2 in the *IRIS HIPPI Administrator's Guide* for more details.

In selecting a mezzanine slot, the following guidelines are suggested:

- If the system has only one IO4 board, this is the location for the mezzanine board. The mezzanine board may be installed in either the upper or lower position on the IO4 board, as illustrated in Figure 2-2.

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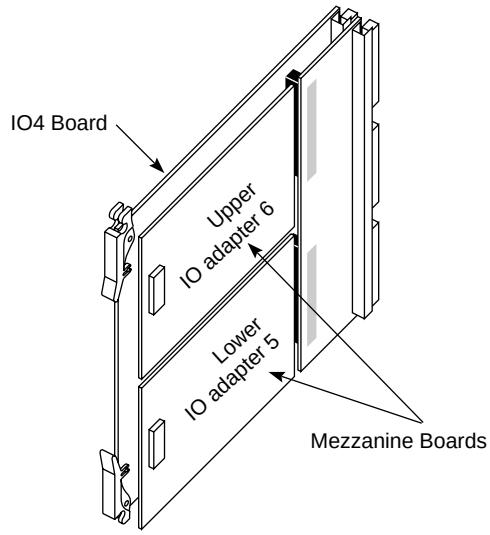

Figure 2-2 Upper and Lower Mezzanine Slots on IO4 Boards

- If the system has more than one IO4 board, select any unoccupied mezzanine slot as close as possible to your selected VMEBus slot. For example, a slot on the IO4 board in slot 5 is preferable to a slot on the IO4 board in slot 4.
- If there are no unoccupied mezzanine slots, you must install another IO4 board. Contact the sales representative to order one. The installation cannot be continued until a mezzanine slot is available.

  Note: The maximum number of IO4 boards for a CHALLENGE Deskside system is three. If three IO4 boards are already installed, and if all the mezzanine slots are occupied, IRIS HIPPI cannot be installed onto this system.

2.1.3 Installing

2.1.3.1 Install Mezzanine Board

Follow the steps below to install the FCI mezzanine card.

1. Remove the IO4 board that you have selected from the CHALLENGE chassis.
2. Lay the board on a flat antistatic surface so that the component side faces up and the SCSI connectors face toward you, as illustrated in Figure 2-3.
3. Locate the selected mezzanine slot (upper or lower) and remove the four screws from the standoffs, as illustrated in Figure 2-3. If the screws are missing, this is not a problem.

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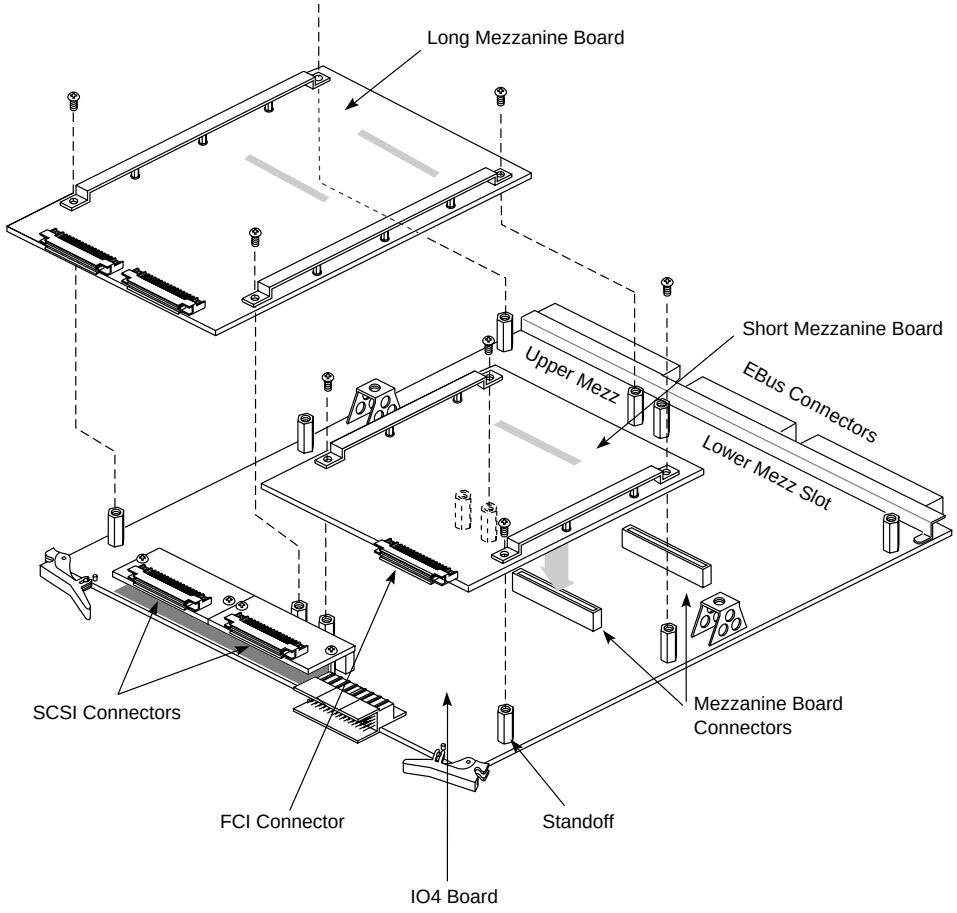

Figure 2-3 IO4 Board with Mezzanine Boards

4. Attach the silver teflon-covered ribbon (FCI) cable to the FCI connector on the mezzanine board.

Caution: The teflon covering on the FCI cable is susceptible to puncturing. Be careful that its installation does not cause it to be pressed or positioned between sharp surfaces (for example, exposed pins).

The cable can be bent, folded, or creased one time without harm. But this type of handling should be done only to position the cable. Repeated handling of this type will break the wires.

5. Position the mezzanine board onto the selected slot so that the connector on the bottom of the mezzanine board matches the mezzanine board receptacle on the IO4 board and the standoffs match the board's holes. Figure 2-3 illustrates the correct positioning for the upper and lower slots.
6. Replace the standoff screws. Use the screws removed previously or the shipped screws. The standoffs have a "float" feature, so the screws do not tighten completely.
7. Create an adapter identification for the mezzanine board. The identification has the format F-*XX*-5 for the lower slot and F-*XX*-6 for the upper slot, where *XX* is the slot number where the IO4 board resides. For example, a mezzanine board in the upper position on the main IO4 board located in slot 5 is labelled F-05-6.
8. From the sheet of labels, remove the two labels with the identification created in the previous step. Attach the larger label to the unattached end of the FCI cable. Attach the smaller-sized label to the outside of the HIPPI I/O panel plate.
9. Reinstall the IO4 board into the chassis, as illustrated in Figure 2-4. Push the board firmly into the backplane. If the board has a VCAM board, the VCAM board must also connect to the backplane.

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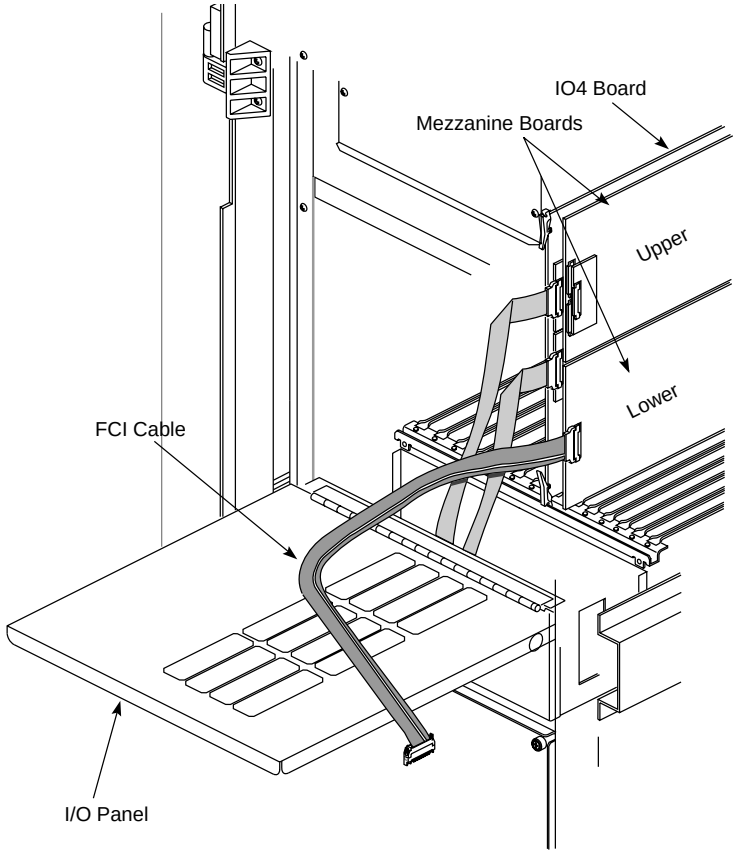

Figure 2-4 Installed IO4 Board

2.1.3.2 Install HIPPI Board

Follow the steps below to install the HIPPI board.

1. Hold the HIPPI board vertically so that the HIPPI and FCI connectors face you, the VMEBus connectors face away from you, and the side of the board with the most components faces to your right, as shown in Figure 2-5.
2. Position the edges of the board into the guides for the selected slot.
3. Slide the HIPPI board into its slot.
4. Push it firmly so that it seats into the backplane.
5. Attach the FCI cable, which was attached in a previous step to the mezzanine board, to the FCI connector on the HIPPI board.

Caution: The teflon covering on the FCI cable is susceptible to puncturing. Be careful that its installation does not cause it to be pressed or positioned between sharp surfaces (for example, exposed pins).
The cable can be bent, folded, or creased one time without harm. But this type of handling should be done only to position the cable. Repeated handling of this type will break the wires.

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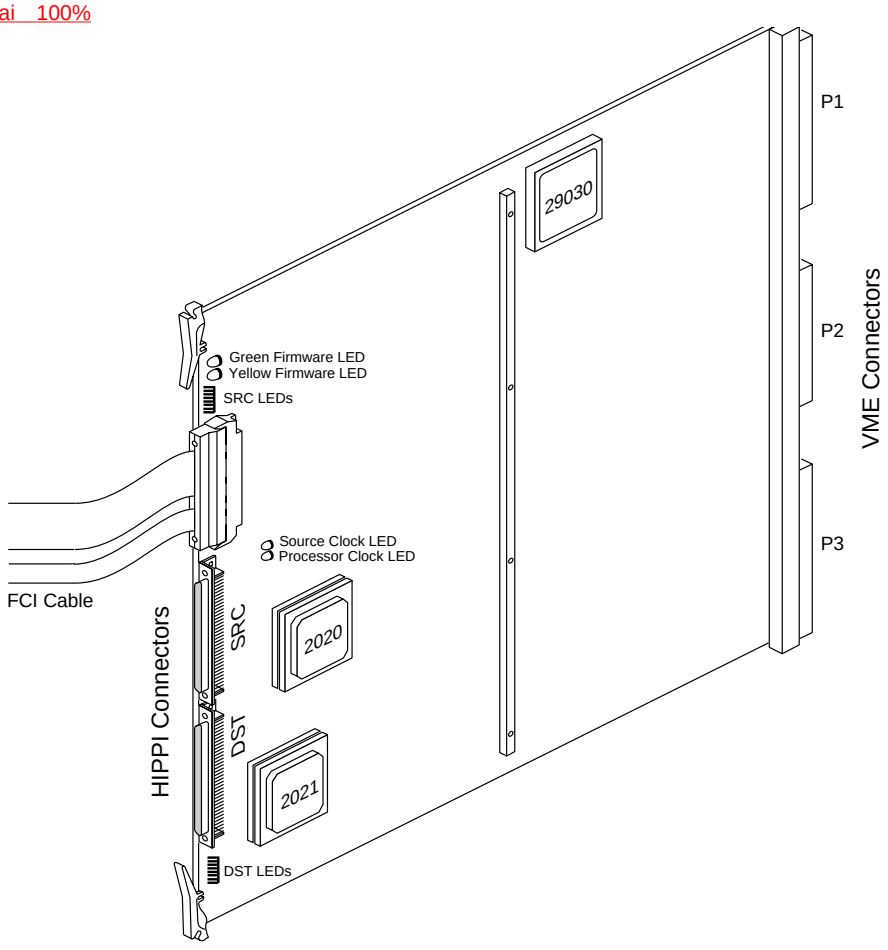

Figure 2-5 IRIS HIPPI Board

2.1.3.3 Connect Internal HIPPI Cables

Follow the steps below to attach the internal HIPPI cables to the HIPPI board and the panel plate to the card cage's I/O panel.

1. Locate the internal cable assembly that consists of the HIPPI I/O panel plate with two internal HIPPI cables attached. The cable assembly is one of the styles shown in Figure 2-6.
2. If the panel plate is not attached to the cables, screw the female connectors of the cables to the panel plate.
3. Remove one blank panel plate from the system's I/O panel and install the HIPPI panel plate.
4. Attach the two internal HIPPI cables to the HIPPI board and screw them into place.
   - The cable labelled **HIPPI DST** (on the panel plate) connects to the bottom connector, located nearest the floor.
   - The cable marked **HIPPI SRC** (on the panel plate) connects to the middle connector, located between the FCI connector and the HIPPI destination connector.
5. Close the I/O door(s) and the chassis doors.

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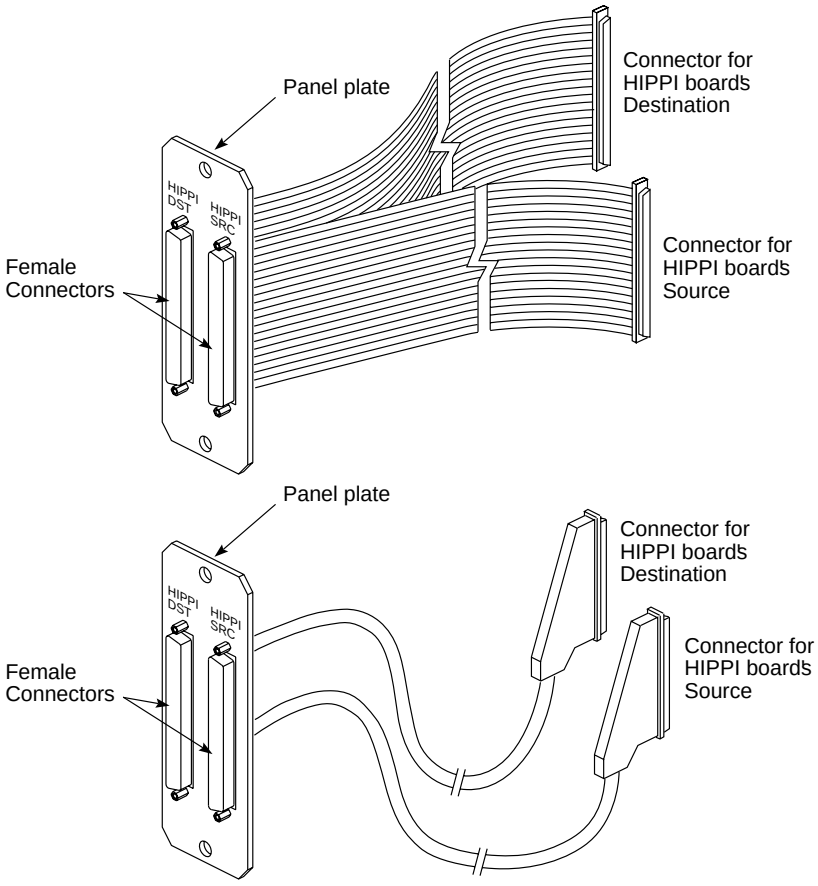

Figure 2-6 Internal HIPPI Cable Assembly (Two Different Styles)

2.1.3.4 Connect Site's HIPPI Cables

Attach the site's HIPPI cables to the system's IRIS HIPPI panel plate, as illustrated in Figure 2-7. Connect the port labelled **HIPPI DST** to the cable from the other system's (or switch's) source port. Attach the port labelled **HIPPI SRC** to the cable from the other system's (or switch's) destination port.

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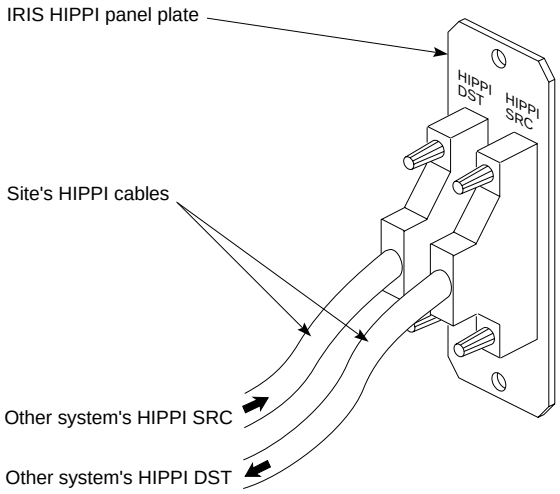

Figure 2-7 Connecting Site HIPPI Cables to Ports on I/O Panel Plate

2.1.4 Completing the Installation

To finish the installation, do the following:

1. Flip the circuit breaker on the back of the chassis to **ON**, then turn the key switch on the front to **ON**.
2. When the console prompts you with the question `Rebuild the operating system?`, answer **`yes`** or **`y`** in order to build a new kernel.

   Note: If this prompt does not appear, you probably have not installed the IRIS HIPPI software. Instead of proceeding with the steps below, follow the instructions in the *IRIS HIPPI Release Notes* to install and configure the software.
3. Logon and reboot (this is the second time you are starting this system) to begin using the newly built operating system. The command lines below can be used to accomplish this step:

   ```
   % su
   Password: thepassword
   # reboot
   ```
4. Logon and invoke */sbin/hinv* to verify that the IRIS HIPPI hardware is listed:

   ```
   % /sbin/hinv
   . . .
   IO4 HIPPI adapter: hippi#, slot # adap #, firmware version ########
   ```

   Note: If the board is not listed, reinstall the product (both boards and all cables) making sure everything is firmly seated and tightly connected.

2.2 Installation for CHALLENGE XL Rackmount System

This section describes the steps for installing the IRIS HIPPI network product into a CHALLENGE XL Rackmount server. The CHALLENGE XL Rackmount platform supports up to four IRIS HIPPI boards.

Warning: **Installing this equipment requires specific training and technical knowledge. These instructions are provided for use only by Silicon Graphics system support engineers (SSEs) or other personnel trained by Silicon Graphics. This equipment uses internal electrical power that is hazardous if the equipment is improperly handled.**

2.2.1 Preparing for Installation

Before starting the installation, prepare yourself and the equipment by following the instructions below.

2.2.1.1 Check the IRIS HIPPI Package for Completeness

Verify that the IRIS HIPPI package is complete. It should contain the items listed in Table 2-3.

Table 2-3 IRIS HIPPI Package Contents

Item	Quantity
Short FCI mezzanine board	1
HIPPI board	1
Teflon-covered FCI (flat cable interface) cable assembly	1
Internal HIPPI cable assembly (includes 2 cables, 4 standoffs, and panel plate)	1
Screws for attaching mezzanine board	4
Labels with adapter IDs	3 sheets
CD-ROM with software (including online release notes)	1
Documentation: *IRIS HIPPI API Programmer's Guide* and *IRIS HIPPI Administrator's Guide*	2 manuals

If anything is missing, do not proceed with the installation. Contact the customer or the customer's salesperson.

2.2.1.2 Prepare the CHALLENGE System

Follow the instructions in this section to prepare the CHALLENGE XL Rackmount system for installation.

Caution: This equipment is extremely sensitive and susceptible to damage by electrostatic discharge (ESD), a spark caused by the buildup of electrical static potential on clothing and other material. You must use proper ESD preventive measures as explained in the "Safety" section of the *CHALLENGE/Onyx XL Rackmount Installation Instructions.*

1. Verify that the IRIX operating system is the correct version for this IRIS HIPPI release using the command below. Do not proceed until the correct version of IRIX is installed, as described in the *IRIS HIPPI Release Notes.*

   ```
   % versions eoe1
   I  eoe1  date  Execution Only Environment 1, version
   ```

2. Verify that the file system is backed up.

3. Optional, but recommended, step.
   Install the IRIS HIPPI software, then do the required configuration steps. Step-by-step instructions are provided in the *IRIS HIPPI Release Notes* and the *IRIS HIPPI Administrator's Guide.* When the software is installed and configured, continue with the next step in these instructions.

   Note: You cannot verify successful installation of the board until the software is installed. If you choose not to install the software now, you will need to do so after the board has been installed.

4. Shut down the system by turning the key on the System Controller panel (located at the front) to **OFF**. Wait a minute for the system to shut down, then switch the power switch on the lower front corner of the chassis to **OFF**.

Warning: Failure to turn off the main power switch may result in electrical shock. Failure to wait for the system to shut down may cause irreparable damage to system components or data.

5. Open the back door and pull down the I/O panel for card cage 2 to expose the IO4 boards and VMEBus slots. If card cage 3 is present, pull down that I/O panel to expose the additional VMEBus slots.

2.2.2 Selecting Mezzanine and VME Slots

To install the IRIS HIPPI network hardware, you need to locate two available slots in the CHALLENGE chassis: one mezzanine slot and one VMEBus slot. Table 2-4 lists the slots from which you can select. It is recommended that the mezzanine and VMEBus slots be as close to each other as possible because the FCI cable will connect them. However, the FCI cable is long enough to accommodate any boards in a properly configured CHALLENGE Rackmount system.

Table 2-4 Slots for IRIS HIPPI Installation in CHALLENGE XL Rackmount System

Slots Required	Slots That Can Be Used
Short mezzanine slot	Upper or lower mezzanine slot on an IO4 board in slot 15, 13, 11, 9, 7, or 5
VMEBus slot	Slot 17, 18, 19, 20, or 21 in card cage 2; or any of slots 2 to 21 in card cage 3

Note: Instead of installing the FMezz board shipped with the IRIS HIPPI product, you may select an FCI connection on an already installed FMezz board (long or short). If you take this option, some of the steps in the section on installing the FMezz board can be skipped; however, other steps are relevant and very important, so do not skip the section.

2.2.2.1 Select a VMEBus Slot

The VMEBus slots of the CHALLENGE XL Rackmount backplane that can be used for IRIS HIPPI are listed in Table 2-4 and illustrated in Figure 2-8 and Figure 2-9. For the HIPPI board, select the first unoccupied slot. Slot 17 is the first VMEBus slot; slot 18 is the second; and so on. If the optional card cage 3 is installed, slot 2 is the first VMEBus slot on the system's second VMEBus, while slot 3 is the second on that bus, and so on.

The following restrictions and guidelines should be followed in making your choice:

- If you select a slot that is not the first available slot on that VMEBus (that is, if you skip a slot within a VMEBus), follow the instructions in the *CHALLENGE/Onyx XL Rackmount Installation Instructions* for jumpering across skipped slots.
- Do not select a VMEBus slot that is reserved for use by a VCAM board (that is, slot 16 in card cage 2 or slot 1 in card cage 3).
- It is possible to install the HIPPI board into a slot that is not serviced by a VCAM board. The VMEBus power module for the slot must be installed, but the VMEBus signals and negative voltages (provided by the VCAM) are not required. For example, you may install the HIPPI board into slot 2 of card cage 3, even if the VCAM in slot 1 is not installed. You will not, however, be able to use subsequent slots of that VMEBus (for example, 3 and 4) for VMEBus operations until a VCAM is installed into the first slot of the bank.

The IRIS HIPPI board typically uses 75 watts of power, drawn from its VMEBus slot. The board requires 5 volts at 15 amps and 12 volts at 1.5 amps. Verify that the slot you have chosen has appropriate power modules installed, and that heat dissipation / ventilation for this card cage can handle this additional board.

Because the IRIS HIPPI board occupies and jumpers a VMEBus slot (just like a normal VMEBus board), regular VMEBus boards may be installed in the slots downstream from the HIPPI board.

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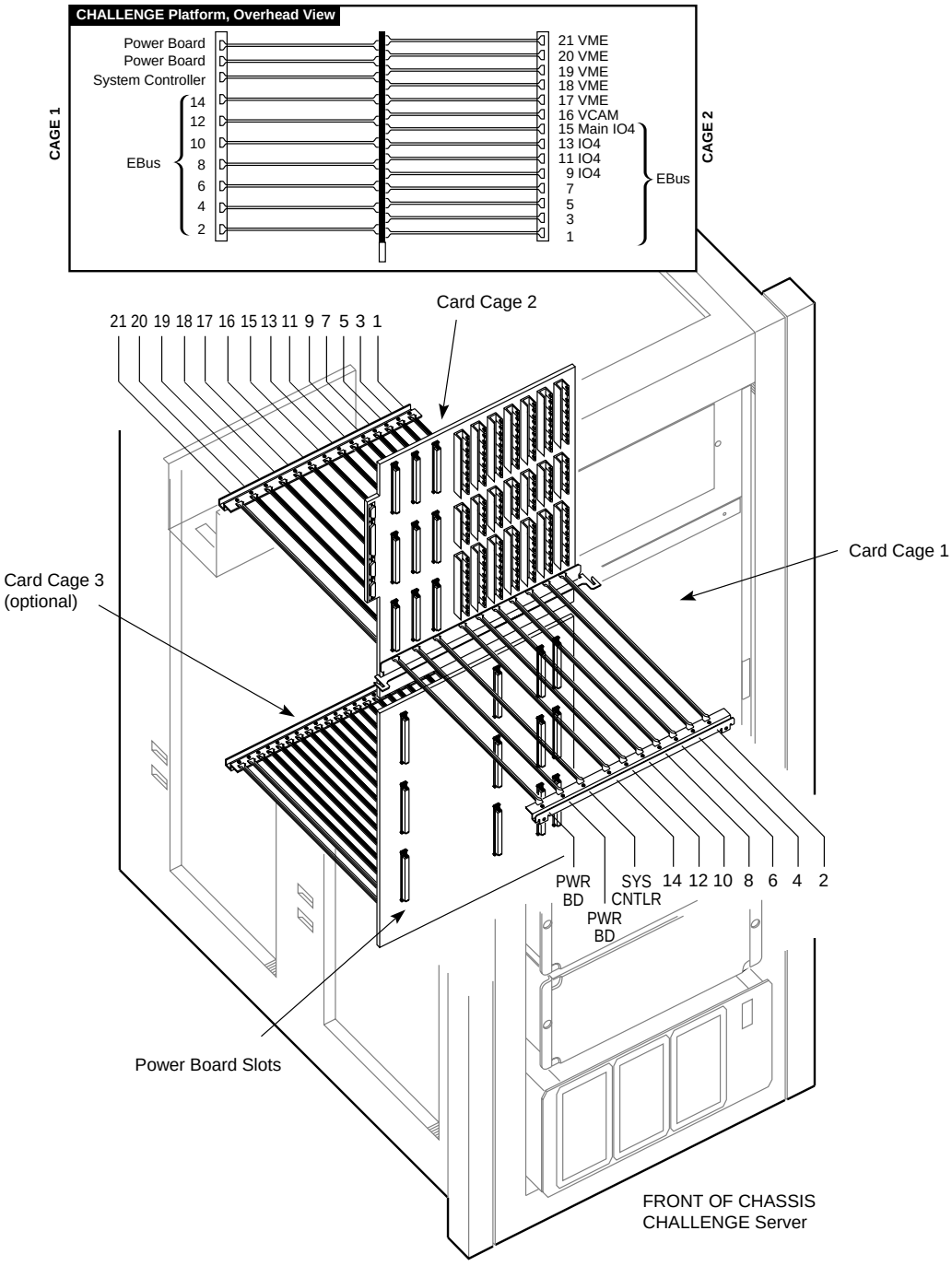

Figure 2-8 CHALLENGE Rackmount Card Cage 2: IO4 and VMEBus Slots

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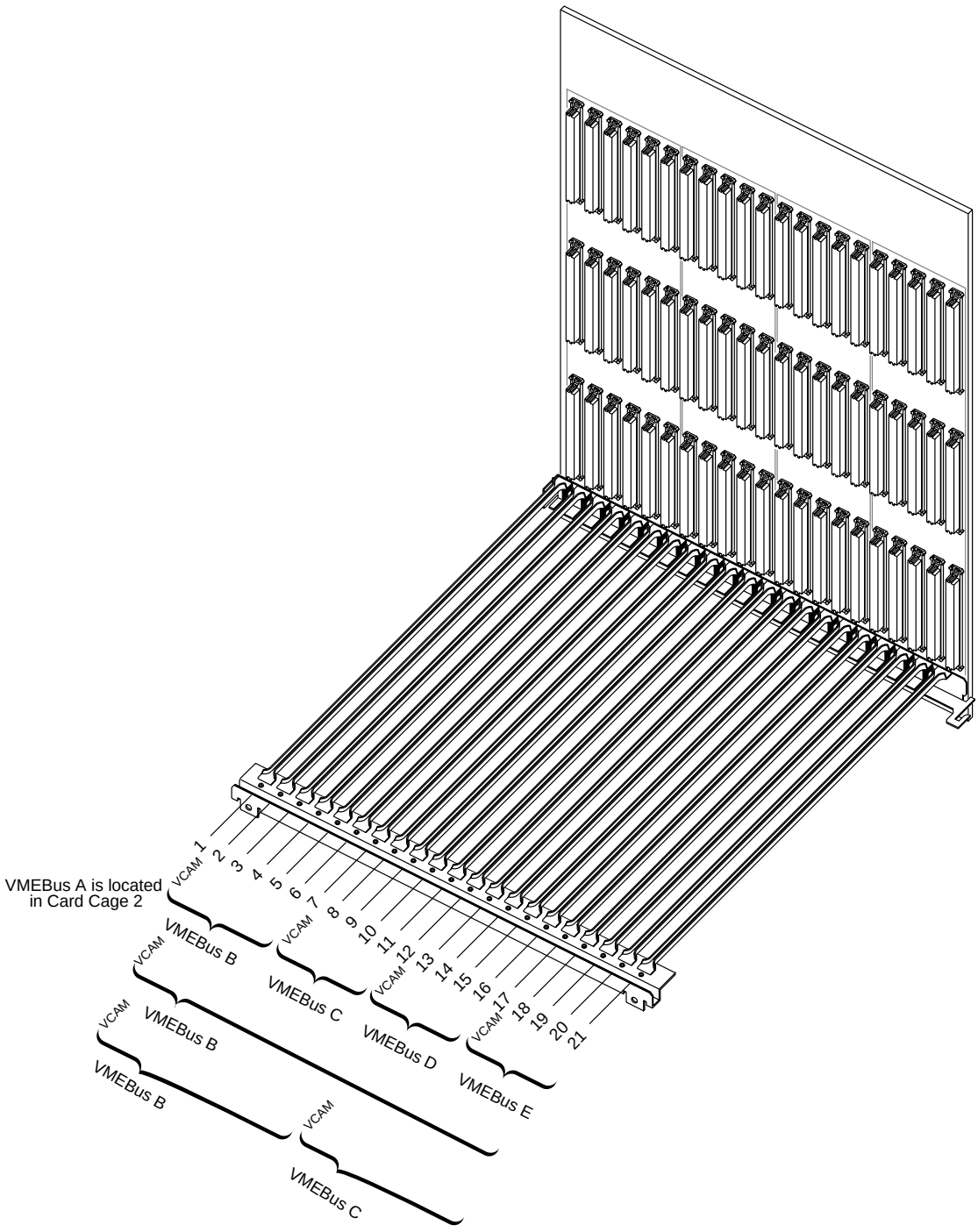

Figure 2-9 CHALLENGE Rackmount Card Cage 3: Additional VMEBus Slots

2.2.2.2 Select a Mezzanine Slot

Locate the IO4 boards that are currently installed. As illustrated in Figure 2-8, slot 15 always has an IO4 board, and slots 13, 11, 9, 7, or 5 may contain IO4 boards. (A CHALLENGE XL Rackmount may have one to six IO4 boards installed.) Two mezzanine slots are located on each IO4 board. The short FCI mezzanine board included in the IRIS HIPPI package may be installed on any of the available mezzanine slots.

Note: When installing an additional IRIS HIPPI network connection, be aware that the ordering of the FMezz boards determines the assignment of IP network interfaces to the IRIS HIPPI boards. During startup, the first FMezz board that is found with a HIPPI board attached is assigned network interface *hip0*; the second is assigned *hip1*, and so on. See Chapter 2 in the *IRIS HIPPI Administrator's Guide* for more details.

In selecting a mezzanine slot, the following guidelines are suggested:

- If the system has only one IO4 board, this is the location for the mezzanine board. The mezzanine board may be installed in either the upper or lower position on the IO4 board. Figure 2-10 illustrates an IO4 board with mezzanine boards in both slots.

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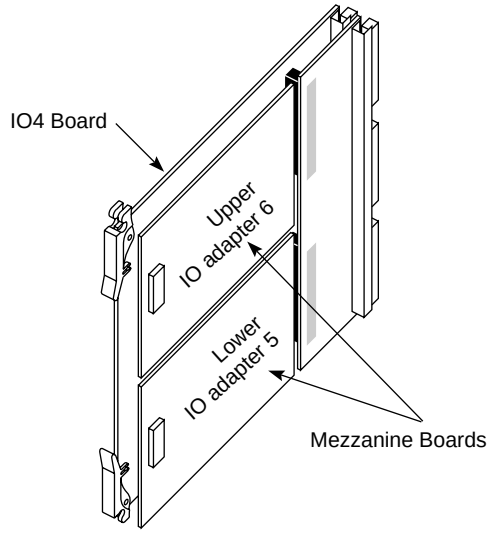

Figure 2-10 Upper and Lower Mezzanine Slots on IO4 Boards

- If the system has more than one IO4 board, select an unoccupied mezzanine slot as close as possible to your selected VMEBus slot. For example, for a VMEBus slot in card cage 2, a slot on the IO4 board in slot 15 is preferable to a slot on the IO4 board in slot 13. However, for a VMEBus slot in card cage 3, a different IO4 board may be a better selection.
- If there are no unoccupied mezzanine slots, you must install another IO4 board. Contact the customer or the customer's sales representative to order one. The installation cannot be continued until a mezzanine slot is available.

  Note: The maximum number of IO4 boards for a CHALLENGE XL Rackmount system is eight. If eight IO4 boards are already installed, and if all the mezzanine slots are occupied, IRIS HIPPI cannot be installed onto this system.

2.2.3 Installing

2.2.3.1 Install Mezzanine Board

Follow the steps below to install the FCI mezzanine card.

1. Remove the IO4 board that you have selected from the CHALLENGE chassis.
2. Lay the board on a flat antistatic surface so that the component side faces up and the SCSII connectors face toward you, as illustrated in Figure 2-11.
3. Locate the selected mezzanine slot (upper or lower) and remove the four screws from the standoffs, as illustrated in Figure 2-11. If the screws are missing, this is not a problem.

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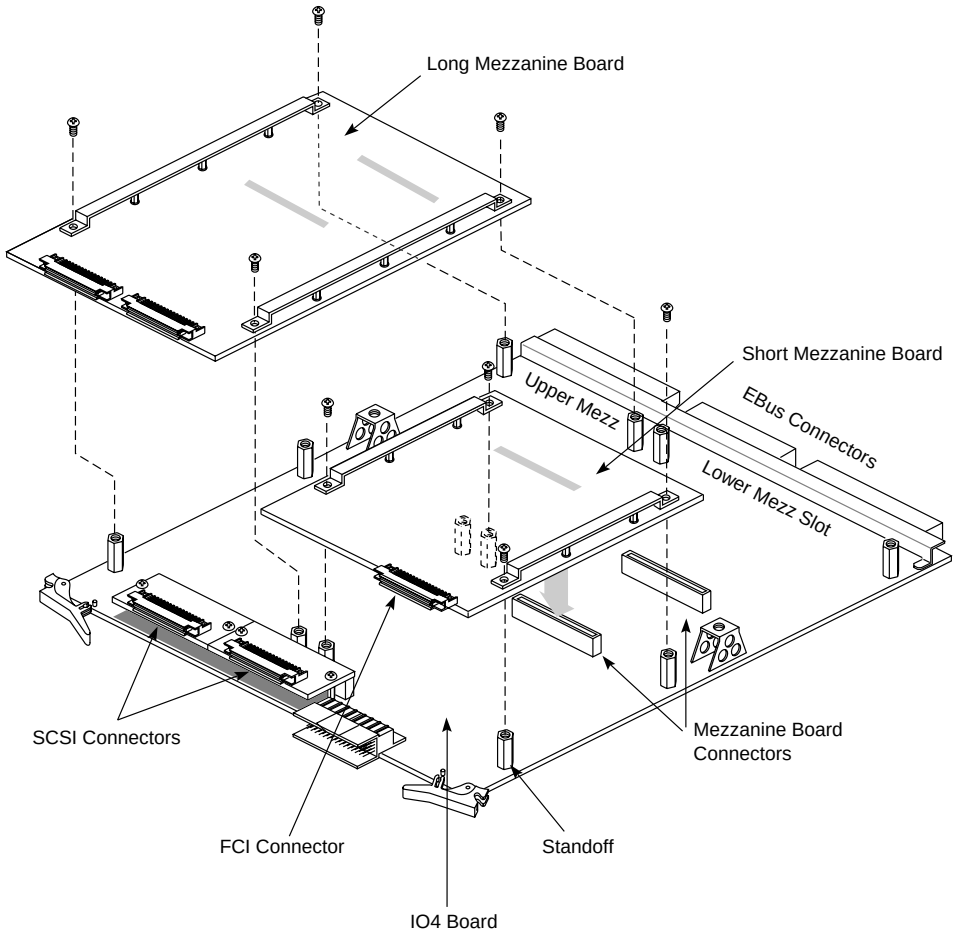

Figure 2-11 IO4 Board with Mezzanine Boards

4. Attach the silver teflon-covered ribbon (FCI) cable to the FCI connector on the mezzanine board.

   Caution: The teflon covering on the FCI cable is susceptible to puncturing. Be careful that its installation does not cause it to be pressed or positioned between sharp surfaces (for example, exposed pins).

The cable can be bent, folded, or creased one time without harm. But this type of handling should be done only to position the cable. Repeated handling of this type will break the wires.

5. Position the mezzanine board onto the selected slot so that the connector on the bottom of the mezzanine board matches the mezzanine board receptacle on the IO4 board and the standoffs match the board's holes. Figure 2-11 illustrates the correct positioning for the upper and lower slots.
6. Replace the standoff screws. Use the screws removed previously or the shipped screws. The standoffs have a "float" feature, so the screws do not tighten completely.
7. Create an adapter identification for the mezzanine board. The identification has the format F-*XX*-5 for the lower slot and F-*XX*-6 for the upper slot, where *XX* is the slot number where the IO4 board resides. For example, a mezzanine board in the upper slot on the main IO4 board located in slot 15 is labelled F-15-6.
8. From the sheet of labels, remove the two labels with the identification created in the previous step. Attach the larger label to the unattached end of the FCI cable. Attach the smaller-sized label to the outside of the HIPPI I/O panel plate.
9. Reinstall the IO4 board into the chassis, as illustrated in Figure 2-12. Push the board firmly into the backplane. If the board has a VCAM board, the VCAM board must also connect to the backplane.

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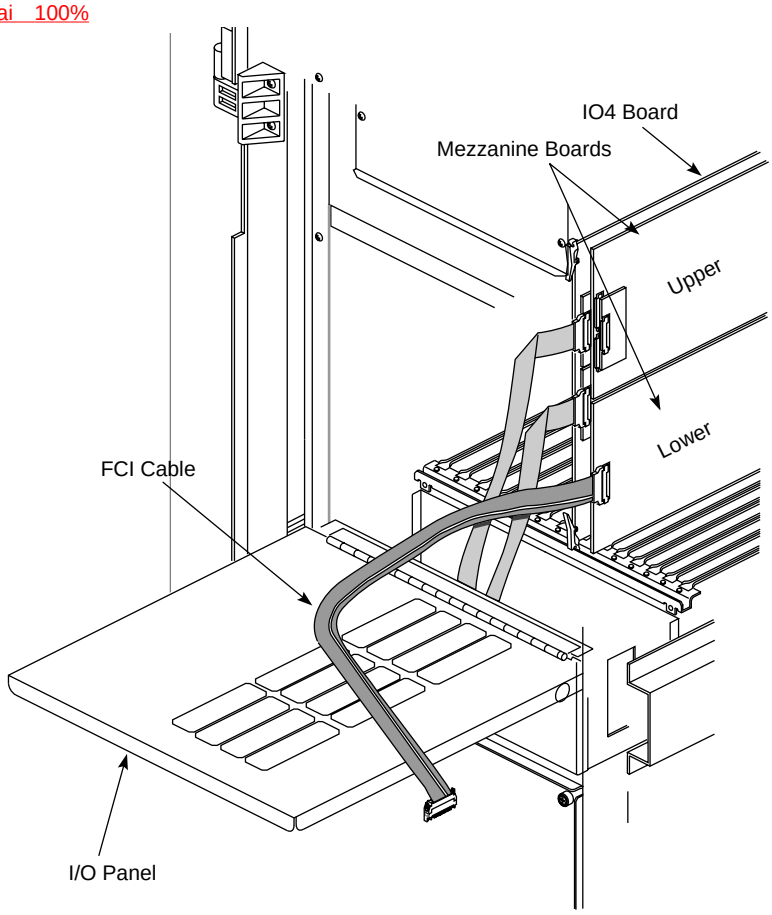

Figure 2-12 Installed IO4 Board

2.2.3.2 Install HIPPI Board

Follow the steps below to install the HIPPI board.

1. Hold the HIPPI board vertically so that the HIPPI and FCI connectors face you, the VMEBus connectors face away from you, and the side of the board with the most components faces to your right, as shown in Figure 2-13.
2. Position the edges of the board into the guides for the selected slot.
3. Slide the HIPPI board into its slot.
4. Push firmly so that it seats into the backplane.
5. Route the FCI cable, which was attached to the mezzanine board in a previous step, through the midplane to the selected VMEBus slot.

   Caution: The teflon covering on the FCI cable is susceptible to puncturing. Be careful that its installation does not cause it to be pressed or positioned between sharp surfaces (for example, exposed pins).
   The cable can be bent, folded, or creased one time without harm. But this type of handling should be done only to position the cable. Repeated handling of this type will break the wires.

6. Attach the FCI cable to the connector on the HIPPI board.

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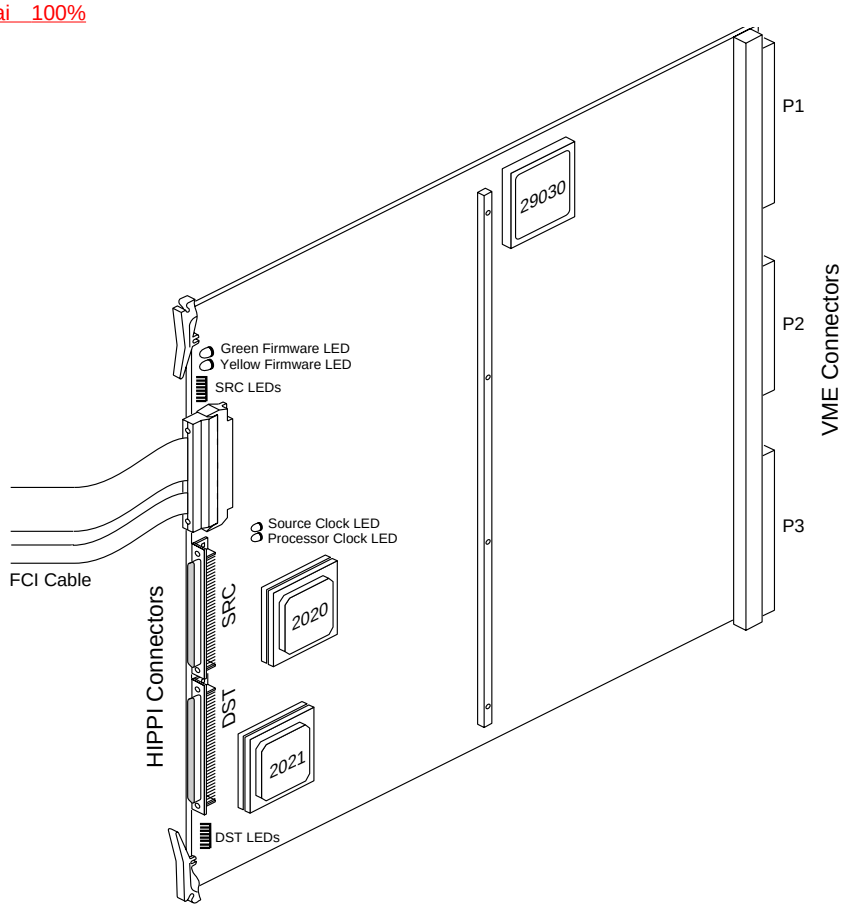

Figure 2-13 IRIS HIPPI Board

2.2.3.3 Connect Internal HIPPI Cables

Follow the steps below to attach the internal HIPPI cables to the HIPPI board and the panel plate to the card cage's I/O panel.

1. Locate the internal cable assembly that consists of the HIPPI I/O panel plate with two internal HIPPI cables attached. The cable assembly is one of the styles shown in Figure 2-14.
2. If the panel plate is not attached to the cables, screw the female connectors of the cables to the panel plate.
3. Remove one blank panel plate from the system's I/O panel and install the HIPPI panel plate.
4. Attach the two internal HIPPI cables to the HIPPI board and screw them into place.
   - The cable labelled **HIPPI DST** (on the panel plate) connects to the bottom connector, located nearest the floor.
   - The cable marked **HIPPI SRC** (on the panel plate) connects to the middle connector, located between the FCI connector and the HIPPI destination connector.
5. Close the I/O door(s) and the chassis doors.

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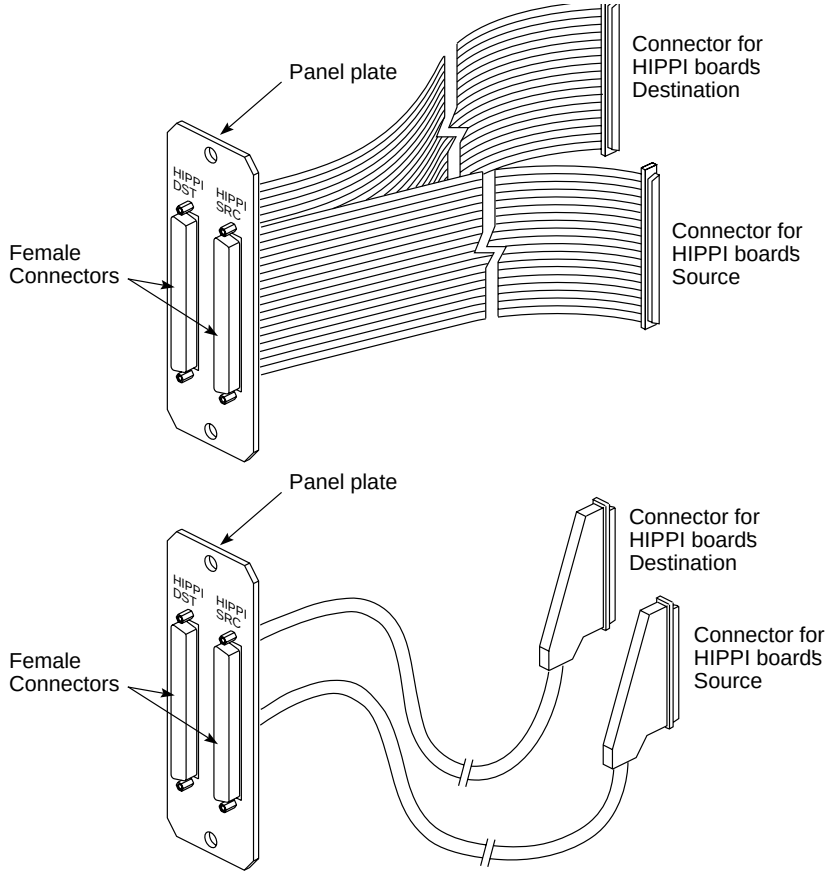

Figure 2-14 Internal HIPPI Cable Assembly (Two Different Styles)

2.2.3.4 Connect Site's HIPPI Cables

Attach the site's HIPPI cables to the system's HIPPI panel plate connectors, as illustrated in Figure 2-15. Connect the I/O port labelled **HIPPI DST** to the cable from the other system's (perhaps switch's) source port. Attach the I/O port labelled **HIPPI SRC** to the cable from the other system's (perhaps switch's) destination port.

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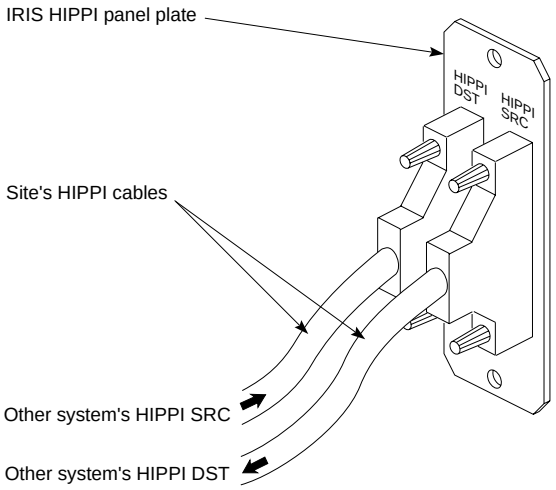

Figure 2-15 Connecting Site HIPPI Cables to Ports on I/O Panel Plate

2.2.4 Completing the Installation

To finish the installation, do the following:

1. Flip the power switch on the front of the chassis to **ON**, then turn the key switch on the front to **ON**.
2. When the console prompts you with the question `Rebuild the operating system?`, answer **yes** or **y** in order to build a new kernel.

   Note: If this prompt does not appear, you probably have not installed the IRIS HIPPI software. Instead of proceeding with the steps below, follow the instructions in the *IRIS HIPPI Release Notes* to install and configure the software.
3. Logon and reboot (this is the second time you are starting this system) to begin using the newly built operating system. The command lines below can be used to accomplish this step:

   ```
   % su
   Password: thepassword
   # reboot
   ```
4. Logon and invoke */sbin/hinv* to verify that the IRIS HIPPI hardware is listed:

   ```
   % /sbin/hinv
   . . .
   IO4 HIPPI adapter: hippi#, slot # adap #, firmware version ########
   ```

   Note: If the board is not listed, reinstall the product (both boards and all cables) making sure everything is firmly seated and tightly connected.

2.3 Installation for Onyx Deskside System

This section describes the steps for installing the IRIS HIPPI network product into an Onyx Deskside server. The Onyx Deskside platform supports up to two IRIS HIPPI boards.

Warning: **Installing this equipment requires specific training and technical knowledge. These instructions are provided for use only by Silicon Graphics system support engineers (SSEs) or other personnel trained by Silicon Graphics. This equipment uses internal electrical power that is hazardous if the equipment is improperly handled.**

2.3.1 Preparing for Installation

Before starting the installation, prepare yourself and the equipment by following the instructions below.

2.3.1.1 Check the IRIS HIPPI Package for Completeness

Verify that the IRIS HIPPI package is complete. It should contain the items listed in Table 2-5. If anything is missing, do not proceed with the installation. Contact the customer or the customer's salesperson.

Table 2-5 IRIS HIPPI Package Contents

Item	Quantity
Short FCI mezzanine board	1
HIPPI board	1
Teflon-covered FCI (flat cable interface) cable assembly	1
Internal HIPPI cable assembly (includes 2 cables, 4 standoffs, and panel plate)	1
Screws for attaching mezzanine board	4
Labels with adapter IDs	3 sheets
CD-ROM with software (including online release notes)	1
Documentation: *IRIS HIPPI API Programmer's Guide* and *IRIS HIPPI Administrator's Guide*	2 manuals

2.3.1.2 Prepare the Onyx System

Follow the instructions in this section to prepare the Onyx Deskside system for installation.

Caution: This equipment is extremely sensitive and susceptible to damage by electrostatic discharge (ESD), a spark caused by the buildup of electrical static potential on clothing and other material. You must use proper ESD preventive measures as explained in the "Safety" section of the *CHALLENGE/Onyx Deskside Installation Instructions*.

1. Verify that the IRIX operating system is the correct version for this IRIS HIPPI release, using the command below. Do not proceed until the correct version of IRIX is installed, as described in the *IRIS HIPPI Release Notes*.

   ```
   % versions eoe1
   I  eoe1  date  Execution Only Environment 1, version
   ```

2. Verify that the file system is backed up.

3. Optional, but recommended, step.
   Install the IRIS HIPPI software, then do the required configuration steps. Step-by-step instructions are provided in the *IRIS HIPPI Release Notes* and the *IRIS HIPPI Administrator's Guide*. When the software is installed and configured, continue with the next step in these instructions.

   Note: You cannot verify successful installation of the board until the software is installed. If you choose not to install the software now, you will need to do so after the board has been installed.

4. Shut down the system by turning the key on the System Controller panel (located at the front) to **OFF**. Wait a minute for the system to shut down, then switch the circuit breaker on the back to **OFF**.

Warning: **Failure to turn off the circuit breaker may result in electrical shock. Failure to wait for the system to shut down may cause irreparable damage to system components or data.**

5. Open the front door and pull down the I/O panel in the front of the chassis to expose the VMEBus slots and IO4 board.

2.3.2 Selecting Mezzanine and VME Slots

To install the IRIS HIPPI network hardware, you need to locate two available slots in the Onyx chassis: one mezzanine slot and one VMEBus slot. Table 2-6 lists the slots from which you can select. It is recommended that the mezzanine and VMEBus slots be as close to each other as possible because the FCI cable will connect them. However, the FCI cable is long enough to accommodate any boards in a properly configured Onyx Deskside system.

Table 2-6 Slots for IRIS HIPPI Installation in Onyx Deskside System

Slots Required	Slots That Can Be Used
Short mezzanine slot	Upper or lower mezzanine slot on IO4 board in slot 3
VMEBus slot	Slot 5, 6, or 7

Note: Instead of installing the FMezz board shipped with the IRIS HIPPI product, you may select an FCI connection on an already installed FMezz board (long or short). If you take this option, some of the steps in the section on installing the FMezz board can be skipped; however, other steps are relevant and very important, so do not skip the section.

2.3.2.1 Select a VMEBus Slot

The VMEBus slots of the Onyx Deskside backplane that can be used for IRIS HIPPI are listed in Table 2-6 and illustrated in Figure 2-16. Select the first unoccupied slot for the HIPPI board. Slot 5 is the first VMEBus slot; slot 6 is the second; and so on.

Note: If you select a slot that is not the first available slot (that is, if you skip a VMEBus slot), follow the instructions in the *CHALLENGE/Onyx Deskside Installation Instructions* for jumpering across skipped slots.

The IRIS HIPPI board typically uses 75 watts of power, drawn from its VMEBus slot. The board requires 5 volts at 15 amps and 12 volts at 1.5 amps. Verify that the slot you have chosen has appropriate power modules installed, and that heat dissipation / ventilation for this card cage can handle this additional board.

Because the IRIS HIPPI board occupies and jumpers a VMEBus slot (just like a normal VMEBus board), regular VMEBus boards may be installed in the slots downstream from the HIPPI board.

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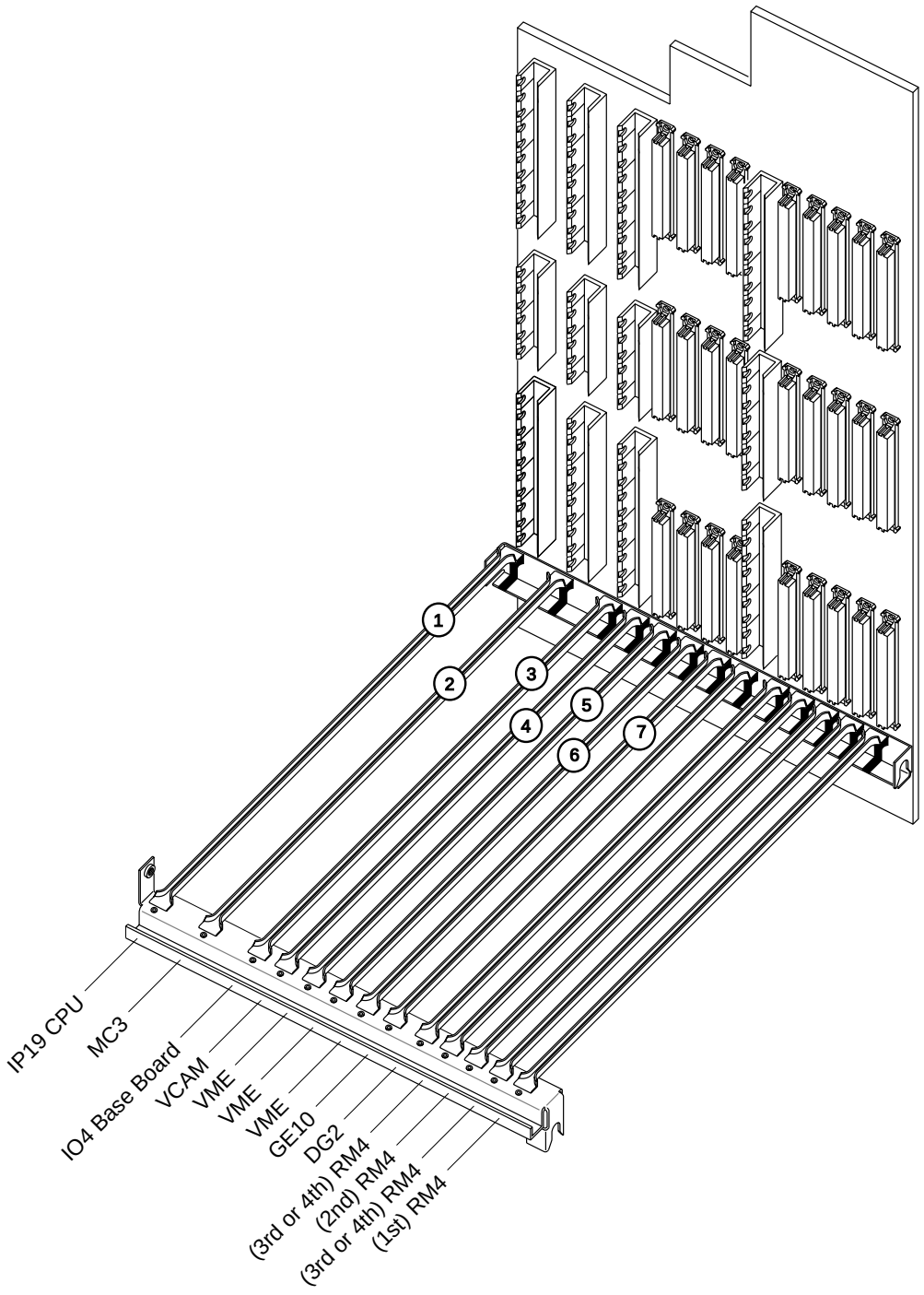

Figure 2-16 Onyx Deskside IO4 and VMEBus Slots

2.3.2.2 Select a Mezzanine Slot

Two short mezzanine slots (upper and lower) are available on the system's IO4 board, as illustrated in Figure 2-17. The short FCI mezzanine board included in the IRIS HIPPI package may be installed on either of these slots. Figure 2-16 shows the IO4 board's location in the Onyx Deskside chassis.

Note: If there are no unoccupied mezzanine slots on this IO4 board, IRIS HIPPI cannot be installed onto this system. The maximum number of IO4 boards for an Onyx Deskside system is one.

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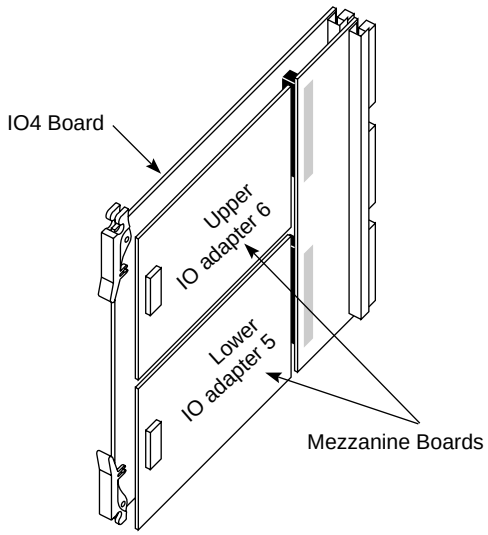

Figure 2-17 Upper and Lower Mezzanine Slots on IO4 Boards

2.3.3 Installing

2.3.3.1 Install Mezzanine Board

Follow the steps below to install the FCI mezzanine card.

1. Remove the IO4 board from the Onyx chassis.
2. Lay the board on a flat antistatic surface so that the component side faces up and the SCSI connectors face toward you, as illustrated in Figure 2-18.
3. Locate the selected mezzanine slot (upper or lower) and remove the four screws from the standoffs, as illustrated in Figure 2-18. If the screws are missing, this is not a problem.

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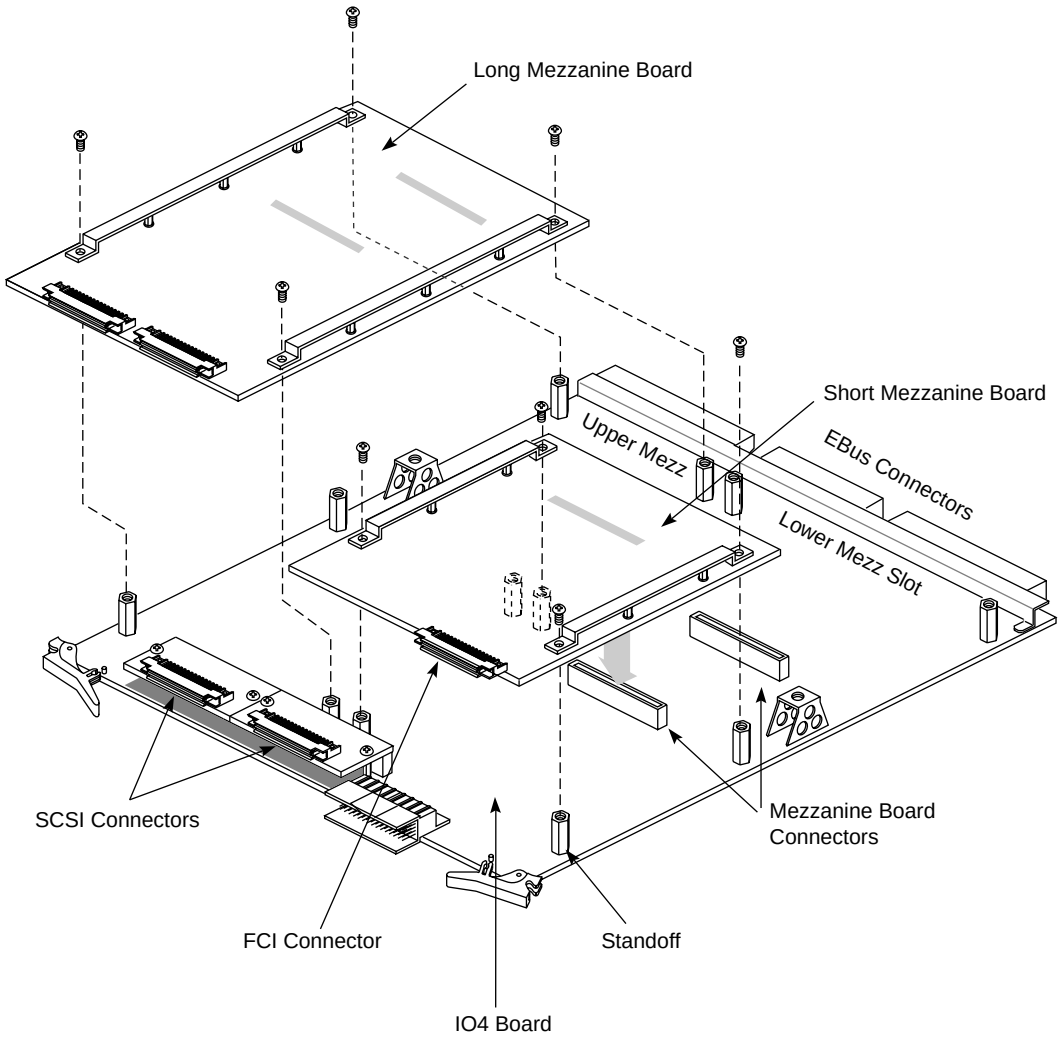

Figure 2-18 IO4 Board with Mezzanine Boards

4. Attach the silver teflon-covered ribbon (FCI) cable to the FCI connector on the mezzanine board.

   Caution: The teflon covering on the FCI cable is susceptible to puncturing. Be careful that its installation does not cause it to be pressed or positioned between sharp surfaces (for example, exposed pins).
   The cable can be bent, folded, or creased one time without harm. But this type of handling should be done only to position the cable. Repeated handling of this type will break the wires.

5. Position the mezzanine board onto the selected slot so that the connector on the bottom of the mezzanine board matches the mezzanine board receptacle on the IO4 board and the standoffs match the board's holes. Figure 2-19 illustrates the correct positioning for the upper and lower slots.

6. Replace the standoff screws. Use the screws removed previously or the shipped screws. The standoffs have a "float" feature, so the screws do not tighten completely.

7. Create an adapter identification for the mezzanine board. The identification is one of the following formats: F-03-5 for the lower slot or F-03-6 for the upper slot
8. From the sheet of labels, remove the two labels with the identification created in the previous step. Attach the larger label to the unattached end of the FCI cable. Attach the smaller-sized label to the outside of the HIPPI I/O panel plate.
9. Reinstall the IO4 board into the chassis, as illustrated in Figure 2-19. Push the board firmly into the backplane. If the board has a VCAM board, the VCAM board must also connect to the backplane.

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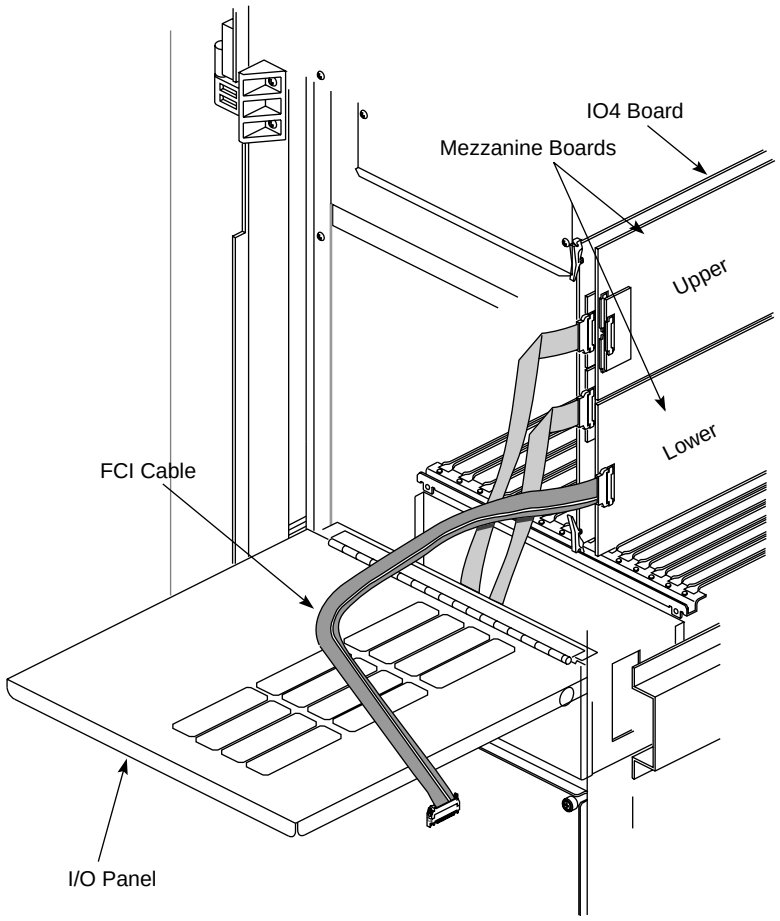

Figure 2-19 Installed IO4 Board

2.3.3.2 Install HIPPI Board

Follow the steps below to install the HIPPI board.

1. Hold the HIPPI board vertically so that the HIPPI and FCI connectors face you, the VMEBus connectors face away from you, and the side of the board with the most components faces to your right, as shown in Figure 2-20.
2. Position the edges of the board into the guides for the selected slot.

3. Slide the HIPPI board into its slot.
4. Push firmly so that it seats into the backplane.
5. Attach the FCI cable, which was attached in a previous step to the mezzanine board, to the FCI connector on the HIPPI board.

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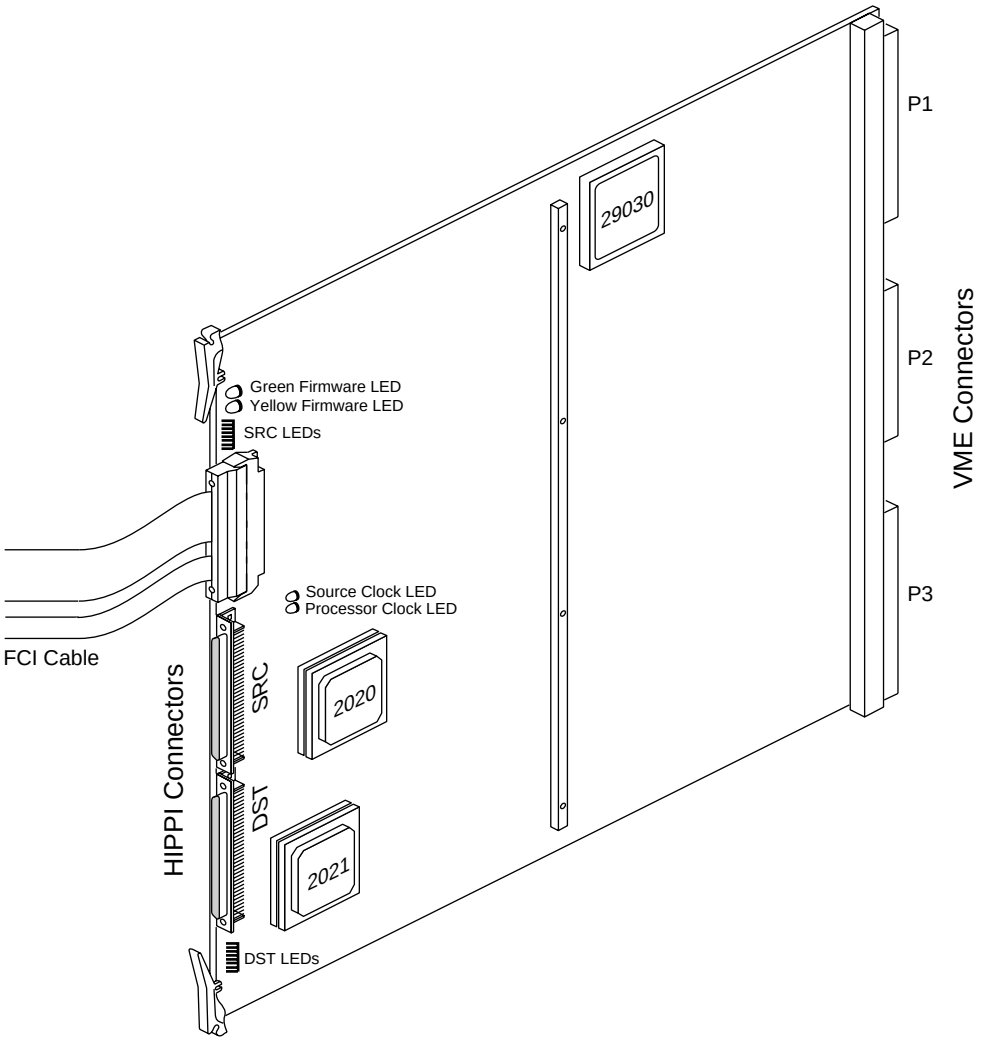

Figure 2-20 IRIS HIPPI Board

2.3.3.3 Connect Internal HIPPI Cables

Follow the steps below to attach the internal HIPPI cables to the HIPPI board and the panel plate to the card cage's I/O panel.

1. Locate the internal cable assembly that consists of the HIPPI I/O panel plate with two internal HIPPI cables attached. The cable assembly is one of the styles shown in Figure 2-21.
2. If the panel plate is not attached to the cables, screw the female connectors of the cables to the panel plate.
3. Remove one blank panel plate from the system's I/O panel and install the HIPPI panel plate.
4. Attach the two internal HIPPI cables to the HIPPI board and screw them into place.
   - The cable labelled **HIPPI DST** (on the panel plate) connects to the bottom connector, located nearest the floor.
   - The cable marked **HIPPI SRC** (on the panel plate) connects to the middle connector, located between the FCI connector and the HIPPI destination connector.
5. Close the I/O door(s) and the chassis doors.

orig/internal.cables.ai 88%

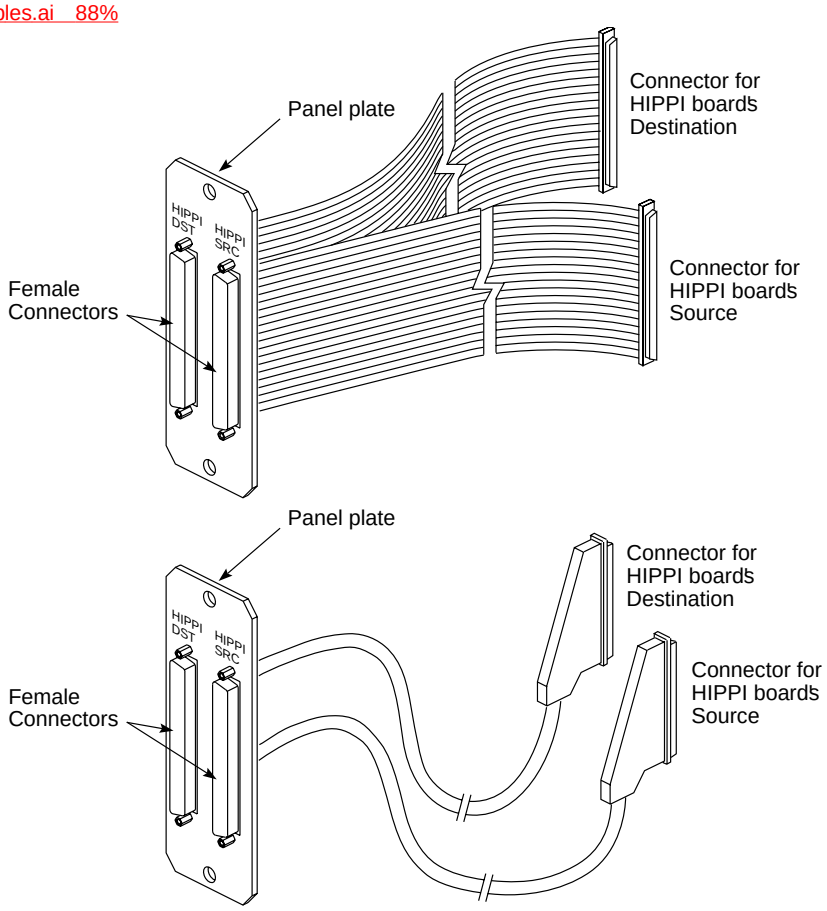

Figure 2-21 Internal HIPPI Cable Assembly (Two Different Styles)

2.3.3.4 Connect Site's HIPPI Cables

Attach the site's HIPPI cables to the system's HIPPI panel plate connectors, as illustrated in Figure 2-22. Connect the port labelled **HIPPI DST** to the cable from the other system's (or switch's) source port. Attach the port labelled **HIPPI SRC** to the cable from the other system's (or switch's) destination port.

orig/iopanel.ai 80%

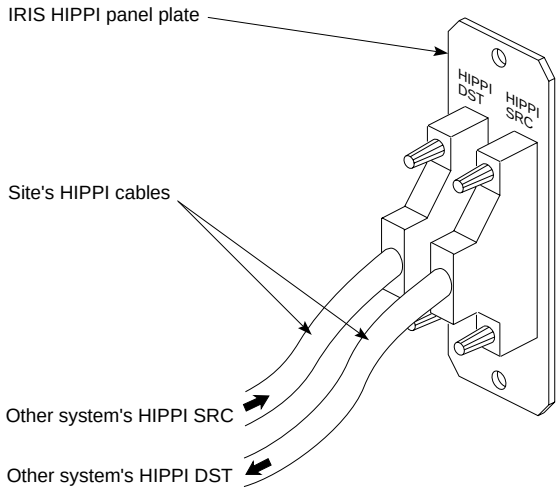

Figure 2-22 Connecting Site HIPPI Cables to Ports on I/O Panel Plate

2.3.4 Completing the Installation

To finish the installation, do the following:

1. Flip the circuit breaker on the back of the chassis to **ON**, then turn the key switch on the front to **ON**.
2. When the console prompts you with the question `Rebuild the operating system?`, answer **yes** or **y** in order to build a new kernel.

   Note: If this prompt does not appear, you probably have not installed the IRIS HIPPI software. Instead of proceeding with the steps below, follow the instructions in the *IRIS HIPPI Release Notes* to install and configure the software.
3. Logon and reboot (this is the second time you are starting this system) to begin using the newly built operating system. The command lines below can be used to accomplish this step:

   ```
   % su
   Password: thepassword
   # reboot
   ```
4. Logon and invoke */sbin/hinv* to verify that the IRIS HIPPI hardware is listed:

   ```
   % /sbin/hinv
   . . .
   IO4 HIPPI adapter: hippi#, slot # adap #, firmware version ########
   ```

   Note: If the board is not listed, reinstall the product (both boards and all cables) making sure everything is firmly seated and tightly connected.

2.4 Installation for Onyx Rackmount System

This section describes the steps for installing the IRIS HIPPI network product into an Onyx Rackmount server. The Onyx Rackmount platform supports up to four IRIS HIPPI boards.

Warning: **Installing this equipment requires specific training and technical knowledge. These instructions are provided for use only by Silicon Graphics system support engineers (SSEs) or other personnel trained by Silicon Graphics. This equipment uses internal electrical power that is hazardous if the equipment is improperly handled.**

2.4.1 Preparing for Installation

Before starting the installation, prepare yourself and the equipment by following the instructions below.

2.4.1.1 Check the IRIS HIPPI Package for Completeness

Verify that the IRIS HIPPI package is complete. It should contain the items listed in Table 2-7. If anything is missing, do not proceed with the installation. Contact the customer or the customer's salesperson.

Table 2-7 IRIS HIPPI Package Contents

Item	Quantity
Short FCI mezzanine board	1
HIPPI board	1
Teflon-covered FCI (flat cable interface) cable assembly	1
Internal HIPPI cable assembly (includes 2 cables, 4 standoffs, and panel plate)	1
Screws for attaching mezzanine board	4
Labels with adapter IDs	3 sheets
CD-ROM with software (including online release notes)	1
Documentation: *IRIS HIPPI API Programmer's Guide* and *IRIS HIPPI Administrator's Guide*	2 manuals

2.4.1.2 Prepare the Onyx System

Follow the instructions in this section to prepare the Onyx Rackmount system for installation.

Caution: This equipment is extremely sensitive and susceptible to damage by electrostatic discharge (ESD), a spark caused by the buildup of electrical static potential on clothing and other material. You must use proper ESD preventive measures as explained in the "Safety" section of the *CHALLENGE/Onyx XL Rackmount Installation Instructions*.

1. Verify that the IRIX operating system is the correct version for this IRIS HIPPI release using the command below. Do not proceed until the correct version of IRIX is installed, as described in the *IRIS HIPPI Release Notes*.

   ```
   % versions eoe1
   I  eoe1  date  Execution Only Environment 1, version
   ```

2. Verify that the file system is backed up.

3. Optional, but recommended, step.
   Install the IRIS HIPPI software, then do the required configuration steps. Step-by-step instructions are provided in the *IRIS HIPPI Release Notes* and the *IRIS HIPPI Administrator's Guide*. When the software is installed and configured, continue with the next step in these instructions.

   Note: You cannot verify successful installation of the board until the software is installed. If you choose not to install the software now, you will need to do so after the board has been installed.

4. Shut down the system by turning the key on the System Controller panel (located at the front) to **OFF**. Wait a minute for the system to shut down, then switch the power switch on the lower front corner of the chassis to **OFF**.

Warning: Failure to turn off the main power switch may result in electrical shock. Failure to wait for the system to shut down may cause irreparable damage to system components or data.

5. Open the back door and pull down the I/O panel for card cage 2 to expose the IO4 boards and VMEBus slots. If card cage 3 is present, pull down that I/O panel to expose the additional VMEBus slots.

2.4.2 Selecting Mezzanine and VME Slots

To install the IRIS HIPPI network hardware, you need to locate two available slots in the Onyx chassis: one mezzanine slot and one VMEBus slot. Table 2-8 lists the slots from which you can select. It is recommended that the mezzanine and VMEBus slots be as close to each other as possible because the FCI cable will connect them. However, the FCI cable is long enough to accommodate any boards in a properly configured Onyx Rackmount system.

Table 2-8 Slots for IRIS HIPPI Installation in Onyx Rackmount System

Slots Required	Slots That Can Be Used
Short mezzanine slot	Upper or lower mezzanine slot on an IO4 board in slot 11, 9, 7, or 5
VMEBus slot	Slot 13, 14, or 15 in card cage 2; or slot 2, 3, 4, 12, 13, or 14 in card cage 3

Note: Instead of installing the FMezz board shipped with the IRIS HIPPI product, you may select an FCI connection on an already installed FMezz board (long or short). If you take this option, some of the steps in the section on installing the FMezz board can be skipped; however, other steps are relevant and very important, so do not skip the section.

2.4.2.1 Select a VMEBus Slot

The VMEBus slots of the Onyx Rackmount backplane that can be used for IRIS HIPPI are listed in Table 2-8 and illustrated in Figure 2-23 and Figure 2-24. For the HIPPI board, select the first unoccupied slot. Slot 13 is the first VMEBus slot; slot 14 is the second; and so on. If the optional card cage 3 is installed, slot 2 is the first VMEBus slot on the system's second VMEBus, while slot 3 is the second on that bus and so on.

The following restrictions and guidelines should be followed in making your choice:

- If you select a slot that is not the first available slot on that VMEBus (that is, if you skip a slot within a VMEBus), follow the instructions in the *CHALLENGE/Onyx XL Rackmount Installation Instructions* for jumpering across skipped slots.
- Do not select a VMEBus slot that is reserved for use by a VCAM board (that is, slot 12 in card cage 2 or slots 1 or 11 in card cage 3).
- It is possible to install the HIPPI board into a slot that is not serviced by a VCAM board. The VMEBus power module for the slot must be installed, but the VMEBus signals and negative voltages (provided by the VCAM) are not required. For example, you may install the HIPPI board into slot 2 of card cage 3, even if the VCAM in slot 1 is not installed. You will not, however, be able to use subsequent slots of that VMEBus (for example, 3 and 4) for VMEBus operations until a VCAM is installed into the first slot of the bank.

The IRIS HIPPI board typically uses 75 watts of power, drawn from its VMEBus slot. The board requires 5 volts at 15 amps and 12 volts at 1.5 amps. Verify that the slot you have chosen has appropriate power modules installed, and that heat dissipation / ventilation for this card cage can handle this additional board.

Because the IRIS HIPPI board occupies and jumpers a VMEBus slot (just like a normal VMEBus board), regular VMEBus boards may be installed in the slots downstream from the HIPPI board.

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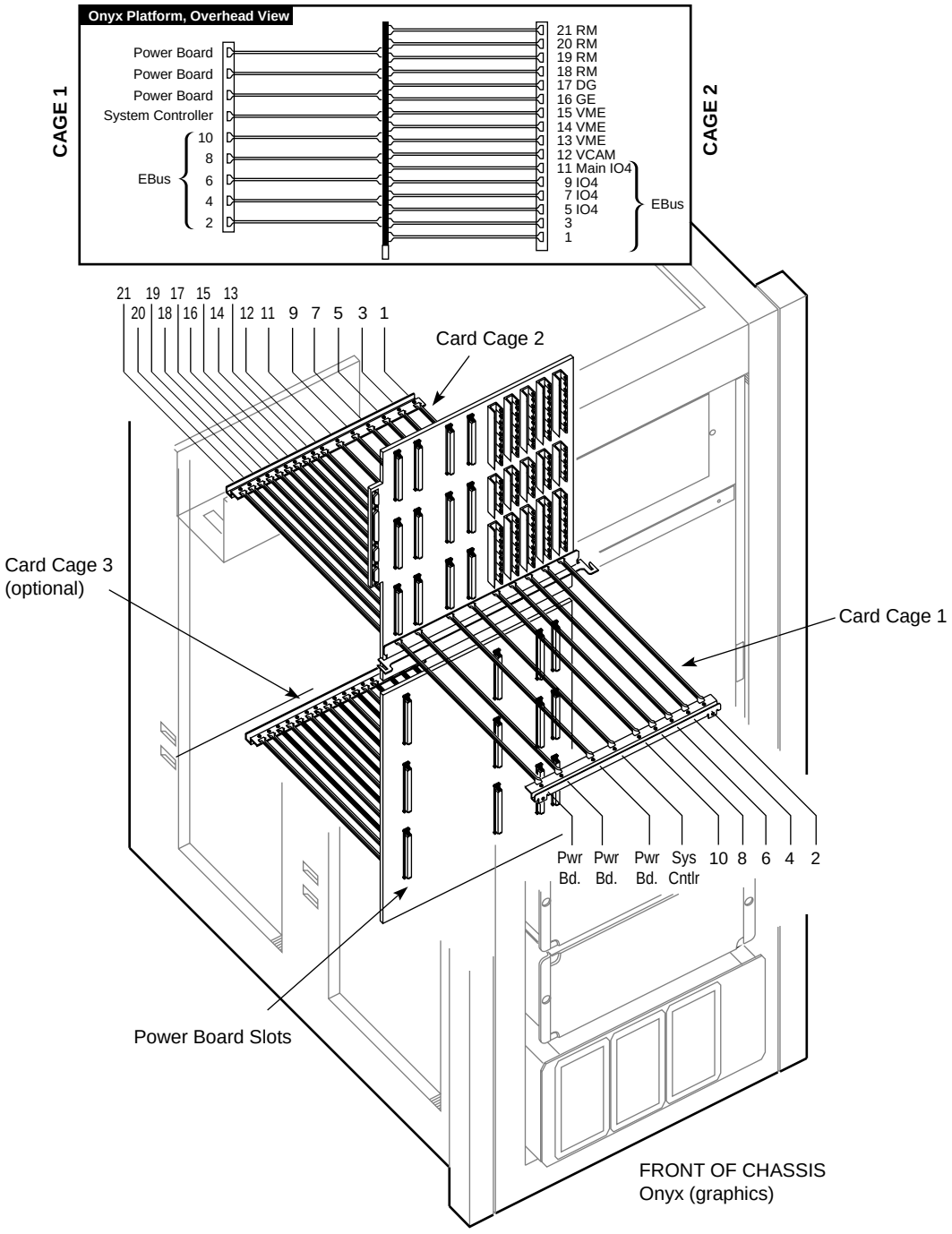

Figure 2-23 Onyx Rackmount Card Cage 2: IO4 and VMEBus Slots

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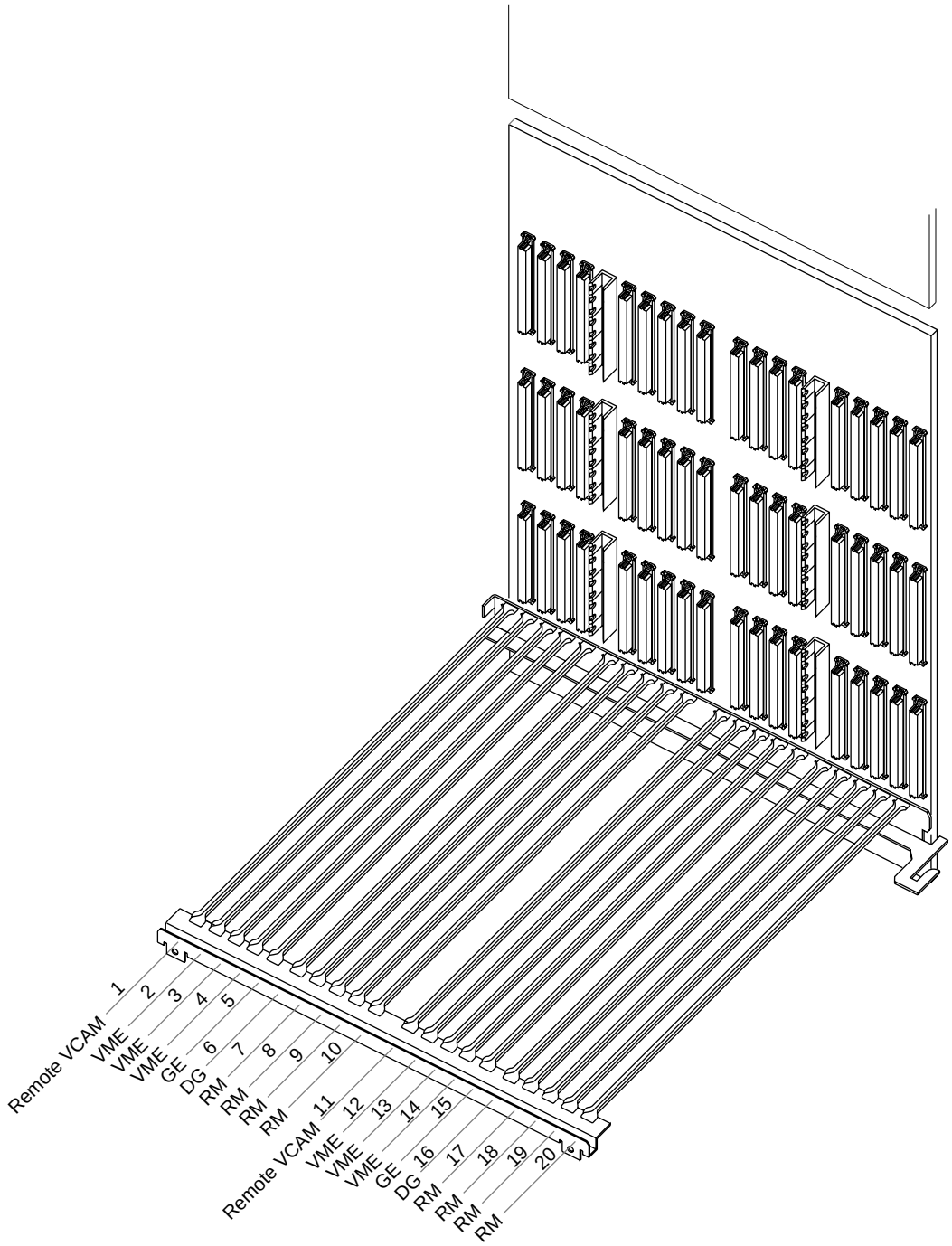

Figure 2-24 Onyx Rackmount Card Cage 3: Additional VMEBus Slots

2.4.2.2 Select a Mezzanine Slot

Locate the IO4 boards currently installed. As illustrated in Figure 2-23, slot 11 always has an IO4 board, and slots 9, 7, or 5 may contain IO4 boards. (An Onyx Rackmount may have one to four IO4 boards installed.) Two mezzanine slots are located on each IO4 board. The short FCI mezzanine board included in the IRIS HIPPI package may be installed on any of the available mezzanine slots.

Note: When installing an additional IRIS HIPPI network connection, be aware that the ordering of the FMezz boards determines the assignment of IP network interfaces to the IRIS HIPPI boards. During startup, the first FMezz board that is found with a HIPPI board attached is assigned network interface *hip0*; the second is assigned *hip1*, and so on. See Chapter 2 in the *IRIS HIPPI Administrator's Guide* for more details.

In selecting a mezzanine slot, the following guidelines are suggested:

- If the system has only one IO4 board, this is the location for the mezzanine board. The mezzanine board may be installed in either the upper or lower position on the IO4 board. Figure 2-25 illustrates an IO4 board with mezzanine boards in both slots.

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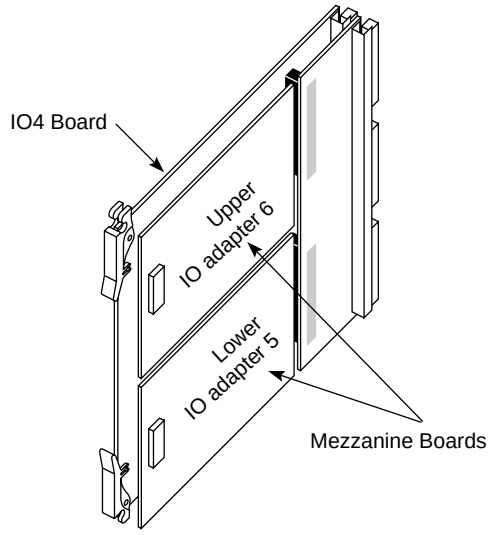

Figure 2-25 Upper and Lower Mezzanine Slots on IO4 Boards

- If the system has more than one IO4 board, select an unoccupied mezzanine slot that is as close as possible to your selected VMEBus slot. For example, for a VMEBus slot in card cage 2, a slot on the IO4 board in slot 11 is preferable to a slot on the IO4 board in slot 19. However, for a VMEBus slot in card cage 3, a different IO4 board may be a better selection.
- If there are no unoccupied mezzanine slots, you must install another IO4 board. Contact the sales representative to order one. The installation cannot be continued until a mezzanine slot is available.

  Note: The maximum number of IO4 boards for an Onyx Rackmount system is six. If six IO4 boards are already installed, and if all the mezzanine slots are occupied, IRIS HIPPI cannot be installed onto this system.

2.4.3 Installing

2.4.3.1 Install Mezzanine Board

Follow the steps below to install the FCI mezzanine card.

1. Remove the IO4 board that you have selected from the Onyx chassis.
2. Lay the board on a flat antistatic surface so that the component side faces up and the SCSI connectors face toward you, as illustrated in Figure 2-26.
3. Locate the selected mezzanine slot (upper or lower) and remove the four screws from the standoffs, as illustrated in Figure 2-26. If the screws are missing, this is not a problem.

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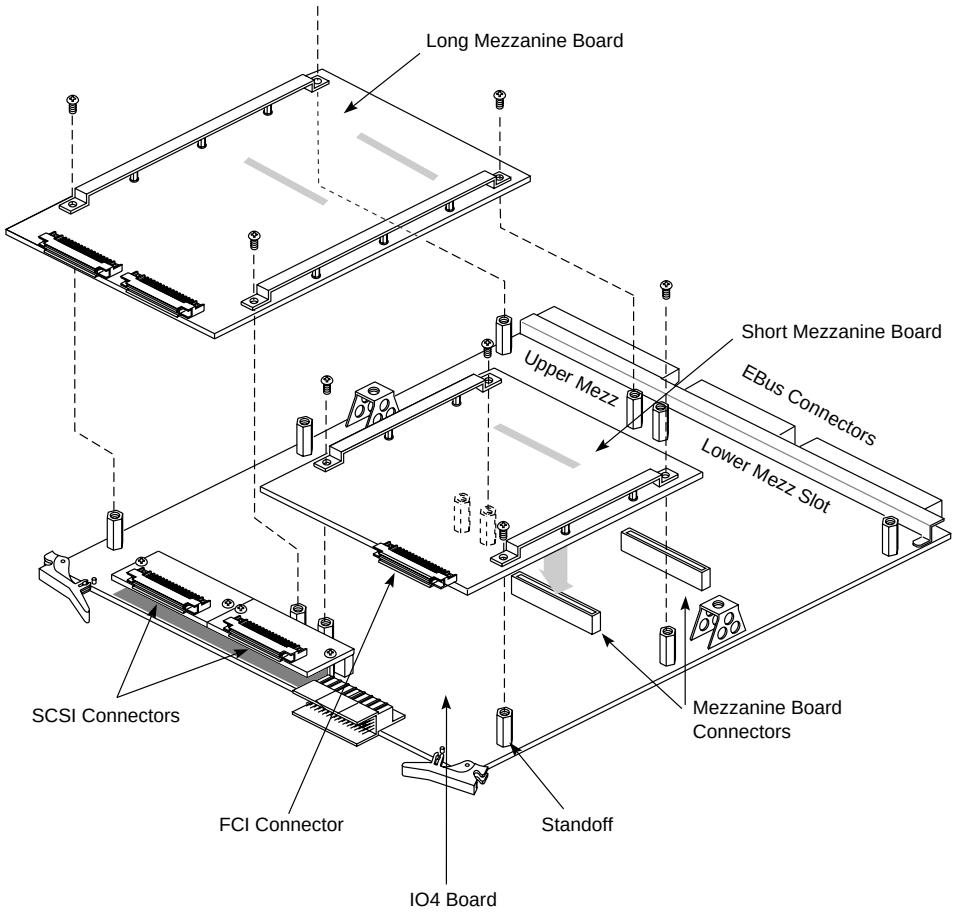

Figure 2-26 IO4 Board with Mezzanine Boards

4. Attach the silver teflon-covered ribbon (FCI) cable to the FCI connector on the mezzanine board.

   Caution: The teflon covering on the FCI cable is susceptible to puncturing. Be careful that its installation does not cause it to be pressed or positioned between sharp surfaces (for example, exposed pins).

The cable can be bent, folded, or creased one time without harm. But this type of handling should be done only to position the cable. Repeated handling of this type will break the wires.

5. Position the mezzanine board onto the selected slot so that the connector on the bottom of the mezzanine board matches the mezzanine board receptacle on the IO4 board and the standoffs match the board's holes. Figure 2-26 illustrates the correct positioning for the upper and lower slots.
6. Replace the standoff screws. Use the screws removed previously or the shipped screws. The standoffs have a "float" feature, so the screws do not tighten completely.
7. Create an adapter identification for the mezzanine board. The identification has the format F-*XX*-5 for the lower slot and F-*XX*-6 for the upper slot, where *XX* is the slot number where the IO4 board resides. For example, a mezzanine board in the upper slot on the main IO4 board located in slot 11 is labelled F-11-6.
8. From the sheet of labels, remove the two labels with the identification created in the previous step. Attach the larger label to the unattached end of the FCI cable. Attach the smaller-sized label to the outside of the HIPPI I/O panel plate.
9. Reinstall the IO4 board into the chassis, as illustrated in Figure 2-27. Push the board firmly into the backplane. If the board has a VCAM board, the VCAM board must also connect to the backplane.

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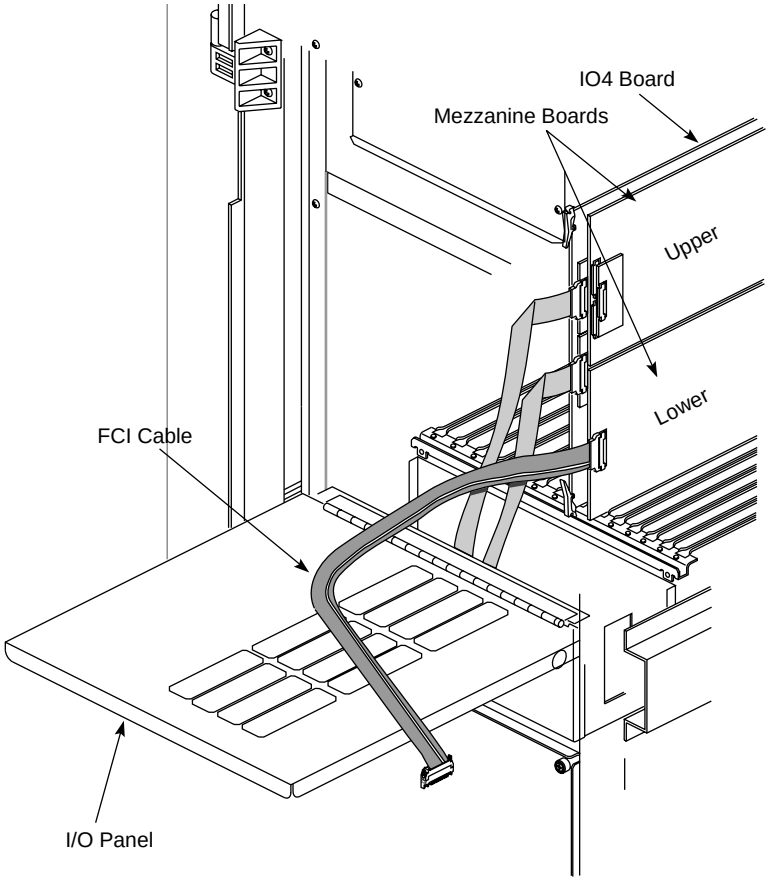

Figure 2-27 Installed IO4 Board

2.4.3.2 Install HIPPI Board

Follow the steps below to install the HIPPI board.

1. Hold the HIPPI board vertically so that the HIPPI and FCI connectors face you, the VMEBus connectors face away from you, and the side of the board with the most components faces to your right, as shown in Figure 2-28.
2. Position the edges of the board into the guides for the selected slot.
3. Slide the HIPPI board into its slot.
4. Push firmly so that it seats into the backplane.
5. Route the FCI cable, which was attached to the mezzanine board in a previous step, through the midplane to the selected VMEBus slot.

   Caution: The teflon covering on the FCI cable is susceptible to puncturing. Be careful that its installation does not cause it to be pressed or positioned between sharp surfaces (for example, exposed pins).
   The cable can be bent, folded, or creased one time without harm. But this type of handling should be done only to position the cable. Repeated handling of this type will break the wires.

6. Attach the FCI cable to the connector on the HIPPI board.

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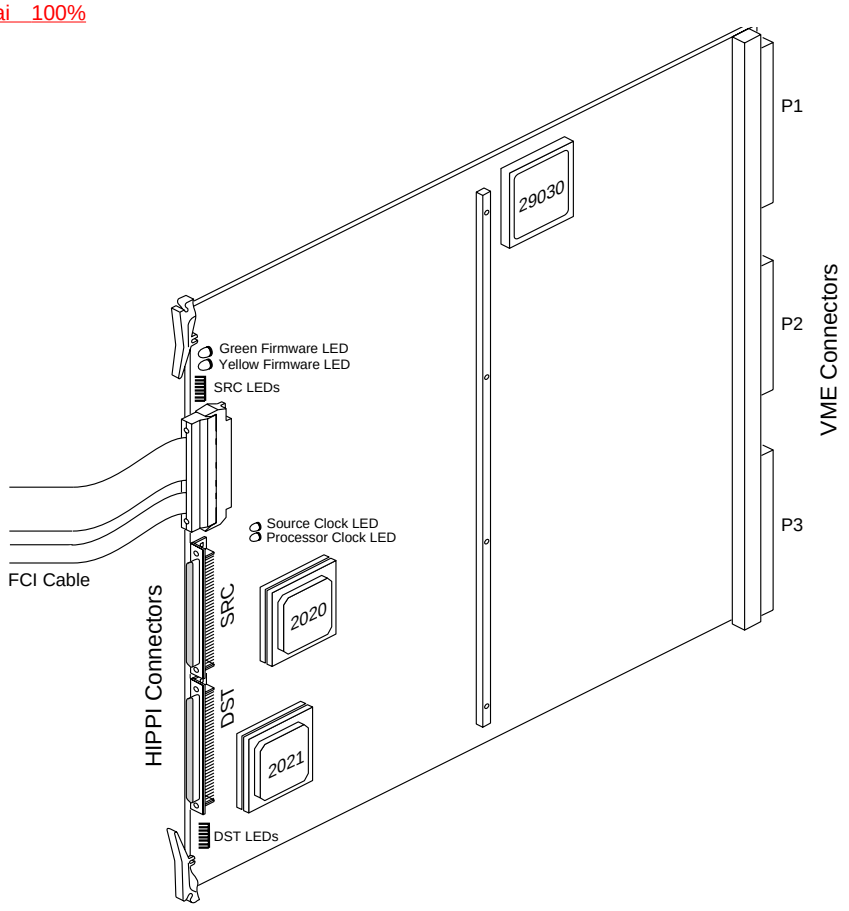

Figure 2-28 IRIS HIPPI Board

2.4.3.3 Connect Internal HIPPI Cables

Follow the steps below to attach the internal HIPPI cables to the HIPPI board and the panel plate to the card cage's I/O panel.

1. Locate the internal cable assembly that consists of the HIPPI I/O panel plate with two internal HIPPI cables attached. The cable assembly is one of the styles shown in Figure 2-29.
2. Remove one blank panel plate from the system's I/O panel and install the HIPPI panel plate.
3. Attach the two internal HIPPI cables to the HIPPI board and screw them into place.
   - The cable labelled **HIPPI DST** (on the panel plate) connects to the bottom connector, located nearest the floor.
   - The cable marked **HIPPI SRC** (on the panel plate) connects to the middle connector, located between the FCI connector and the HIPPI destination connector.
4. Close the I/O door(s) and the chassis doors.

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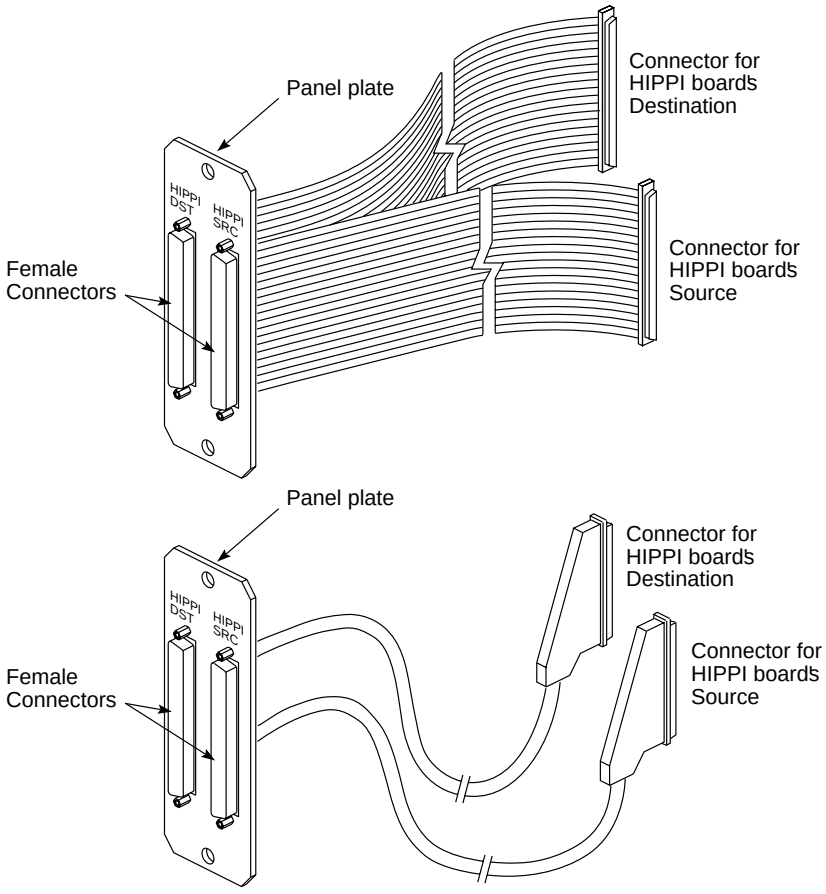

Figure 2-29 Internal HIPPI Cable Assembly (Two Different Styles)

2.4.3.4 Connect Site's HIPPI Cables

Attach the site's HIPPI cables to the system's HIPPI panel plate connectors, as illustrated in Figure 2-30. Connect the I/O port labelled **HIPPI DST** to the cable from the other system's (perhaps switch's) source port. Attach the I/O port labelled **HIPPI SRC** to the cable from the other system's (perhaps switch's) destination port.

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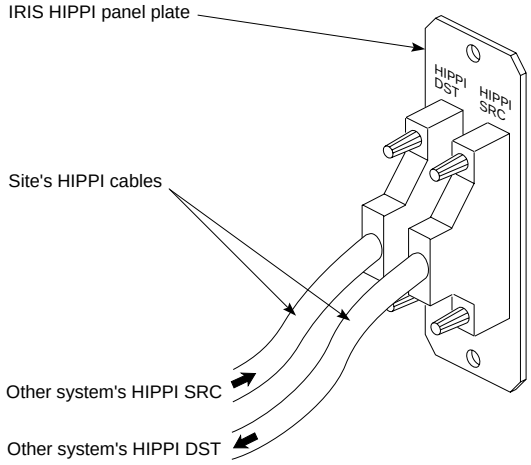


Figure 2-30 Connecting Site HIPPI Cables to Ports on I/O Panel Plate

2.4.4 Completing the Installation

To finish the installation, do the following:

1. Flip the power switch on the front of the chassis to **ON**, then turn the key switch on the front to **ON**.
2. When the console prompts you with the question `Rebuild the operating system?`, answer **yes** or **y** in order to build a new kernel.

   Note: If this prompt does not appear, you probably have not installed the IRIS HIPPI software. Instead of proceeding with the steps below, follow the instructions in the *IRIS HIPPI Release Notes* to install and configure the software.
3. Logon and reboot (this is the second time you are starting this system) to begin using the newly built operating system. The command lines below can be used to accomplish this step:

   ```
   % su
   Password: thepassword
   # reboot
   ```
4. Logon and invoke */sbin/hinv* to verify that the IRIS HIPPI hardware is listed:

   ```
   % /sbin/hinv
   . . .
   IO4 HIPPI adapter: hippi#, slot # adap #, firmware version ########
   ```

   Note: If the board is not listed, reinstall the product (both boards and all cables) making sure everything is firmly seated and tightly connected.

Chapter 3

IRIS HIPPI LEDs

This chapter describes how the IRIS HIPPI light-emitting diodes (LEDs) behave.

3.1 Summary of LEDs on IRIS HIPPI Board

The lRIX HIPPI board has the following LEDs, which are described in separate sections below:

- one green and one yellow, controlled by the firmware
- two small red, controlled by the board's processor and source clocks
- eight red, controlled by the destination channel (AMCC 2021 component)
- eight red, controlled by the source channel (AMCC 2020 component)

3.2 Green and Yellow LEDs

The green and yellow LEDs are controlled by the IRIS HIPPI board's firmware.

The yellow and green LEDs both blink steadily when there is power to the board and the UNIX initialization scripts the have not run to completion. Once the initialization process is complete, the yellow LED is off.

The green LED blinks steadily when there is power to the board and the board's initialization procedures have successfully brought the board into operation.

The yellow LED blinks alone when there is a problem. If the IRIS HIPPI board's firmware fails, the firmware attempts to determine the reason for the failure and to communicate the reason by blinking a code on the yellow LED. The codes are summarized in Table 3-3.

See sections 3.6 (normal operation) and 3.7 (problematic behavior) for full descriptions of the behavior for these LEDs.

3.3 Clock LEDs

The two small red LEDs labelled PCLK and SCLK are steadily on when the clocks for the respective components are functioning. The LED labelled PCLK is for the IRIS HIPPI board's processor (AMD 29030 component); the one labelled SCLK is for the source component (AMCC 2020 component).

If either of these LEDs is off, the associated component is not operational and the IRIS HIPPI board is dysfunctional, in which case you should contact the Silicon Graphics Technical Assistance Center.

3.4 Destination LEDs

Each of the eight red destination LEDs blinks to indicate a particular event on the IRIS HIPPI board. Figure 3-1 describes what one blink of each LED means. Figure 3-1 illustrates the events that cause each LED to blink. Some of the events are the assertion of a HIPPI-PH signal as detected on one of the AMCC 2021 pins, others are the assertion of an input pin from the IRIS HIPPI board's logic.

Table 3-1 Destination LEDs

Label on IRIS HIPPI Board	Description of LED
DSIC	2021's DST to SRC Interconnect output pin. When this LED is on, the IRIS HIPPI board's destination is online and asserting its HIPPI-PH Destination-to-Source **INTERCONNECT** signal. It is not in test mode. That is, this end (the destination) of the link is available for "action."
SRCAV	2021's Source Available (SRCAV) output pin. When this LED is on, the other end is online and asserting its HIPPI-PH Source-to-Destination **INTERCONNECT** signal. That is, the other end of the link is available for "action."
CONRQ	2021's Connect Request (CONRQ) output pin. When this LED is on, the 2021 is detecting an asserted HIPPI-PH connection **REQUEST** signal, indicating that a HIPPI end source is requesting that a connection be opened.
CONIN	2021's Connect In (CONIN) input pin. When this LED is on, the firmware is programming the 2021 to assert the HIPPI-PH **CONNECT** (response) signal. This indicates that the board has accepted a connection request. When both CONRQ and CONIN LEDs are on, a connection is open.

Table 3-1 (continued) Destination LEDs

Label on IRIS HIPPI Board	Description of LED
RDYIN	2021's Ready In (RDYIN) input pin. When this LED is on, the firmware is telling the 2021 to send (or store up, if there is not an active connection) a HIPPI-PH **READY** pulse. Each blink increments the destination's READY counter by one and, if there is an open connection, causes a **READY** pulse to be sent to the source. There is a 1.5-millisecond pulse stretcher on this LED to ensure that the blink is visible.
PKOUT	2021's Packet Out (PKOUT) output pin. When this LED is on, the 2021 is detecting an asserted HIPPI-PH **PACKET** signal. This indicates that the source is sending a packet.
BROUT	2021's Burst Out (BROUT) output pin. When this LED is on, the 2021 is detecting an asserted HIPPI-PH **BURST** signal. This indicates that the source is sending a burst.
ERROR	2021's Error output pin, indicating that one of the following events occurred: 2021-reported Sequence Error 2021-reported Parity Error 2021-reported LLRC Error 2021-reported Sync Error Illegal Burst Error (can be any of the following): Two short bursts in one packet. A short burst that is not the first or last. A burst consisting of more than 256 words. There is a 1.5-millisecond pulse stretcher on this LED to ensure that the blink is visible.

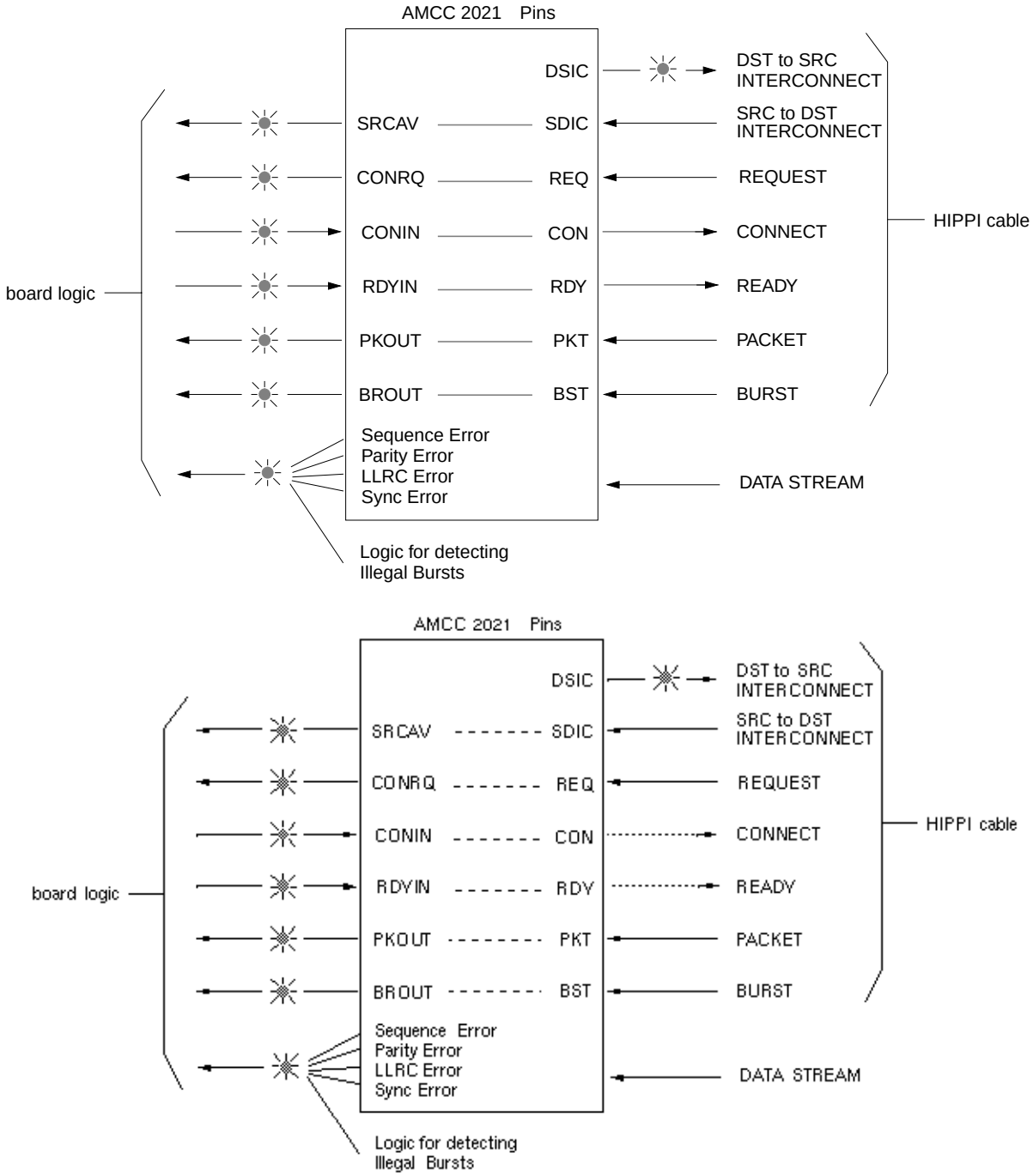


Figure 3-1 Signals That Control Destination LEDs

3.5 Source LEDs

Each of the eight red source LEDs blinks to indicate a particular event on the IRIS HIPPI board. Table 3-2 describes what one blink of each LED means. Figure 3-2 illustrates the events that cause each LED to blink. Some of the events are the assertion of a HIPPI-PH signal as detected on one of the AMCC 2020 pins; others are the assertion of an input pin from the IRIS HIPPI board's logic.

Table 3-2 Source LEDs

Label on IRIS HIPPI Board	Description of LED
SDIC	2020's SRC to DST Interconnect output pin. When this LED is on, the IRIS HIPPI board's source is online and asserting its HIPPI-PH Source-to-Destination **INTERCONNECT** signal. It is not in test mode. That is, this end (the source) of the link is available for "action."
DSTAV	2020's Destination Available (DSTAV) output pin. When this LED is on, the other end is online and asserting its HIPPI-PH Destination-to-Source **INTERCONNECT** signal. That is, the other end of the link is available for "action."
CNREQ	2020's Connect Request (CNREQ) input pin. When this LED is on, the host / firmware is telling the 2020 to take the provided I-field and assert the HIPPI-PH connection **REQUEST** signal. The 2020 is probably asserting the **REQUEST** signal.
CNOUT	2020's Connect Out (CNOUT) output pin. When this LED is on, the 2020 is detecting an asserted HIPPI-PH **CONNECT** signal, indicating that the connection to the destination is open.
DTREQ	2020's Data Request (DTREQ) output pin. When this LED is on, the destination is waiting for more data. This LED is on whenever there is an open connection and the source has received at least one **READY** signal for which it has not yet sent a burst (that is, the source's READY counter is greater than zero). There is a 1.5-millisecond pulse stretcher on this LED to ensure that the blink is visible.
PKTAV	2020's Packet Available (PKTAV) input pin. When this LED is on, the firmware is programming the 2020 to send a packet. If it can (for example, if a connection is open), the 2020 is asserting the HIPPI-PH **PACKET** signal on the HIPPI channel.
BSTAV	2020's Burst Available (BSTAV) and Data Available (DATAV) input pins. When this LED is on, the board has data to send. If it can, the 2020 will assert the HIPPI-PH **BURST** signal on the HIPPI channel.
ERROR	One of the following events occurred: 2020-reported Sequence Error A destination actively rejected a connection request 2020-reported Parity Error There is a 1.5-millisecond pulse stretcher on this LED to ensure that the blink is visible.

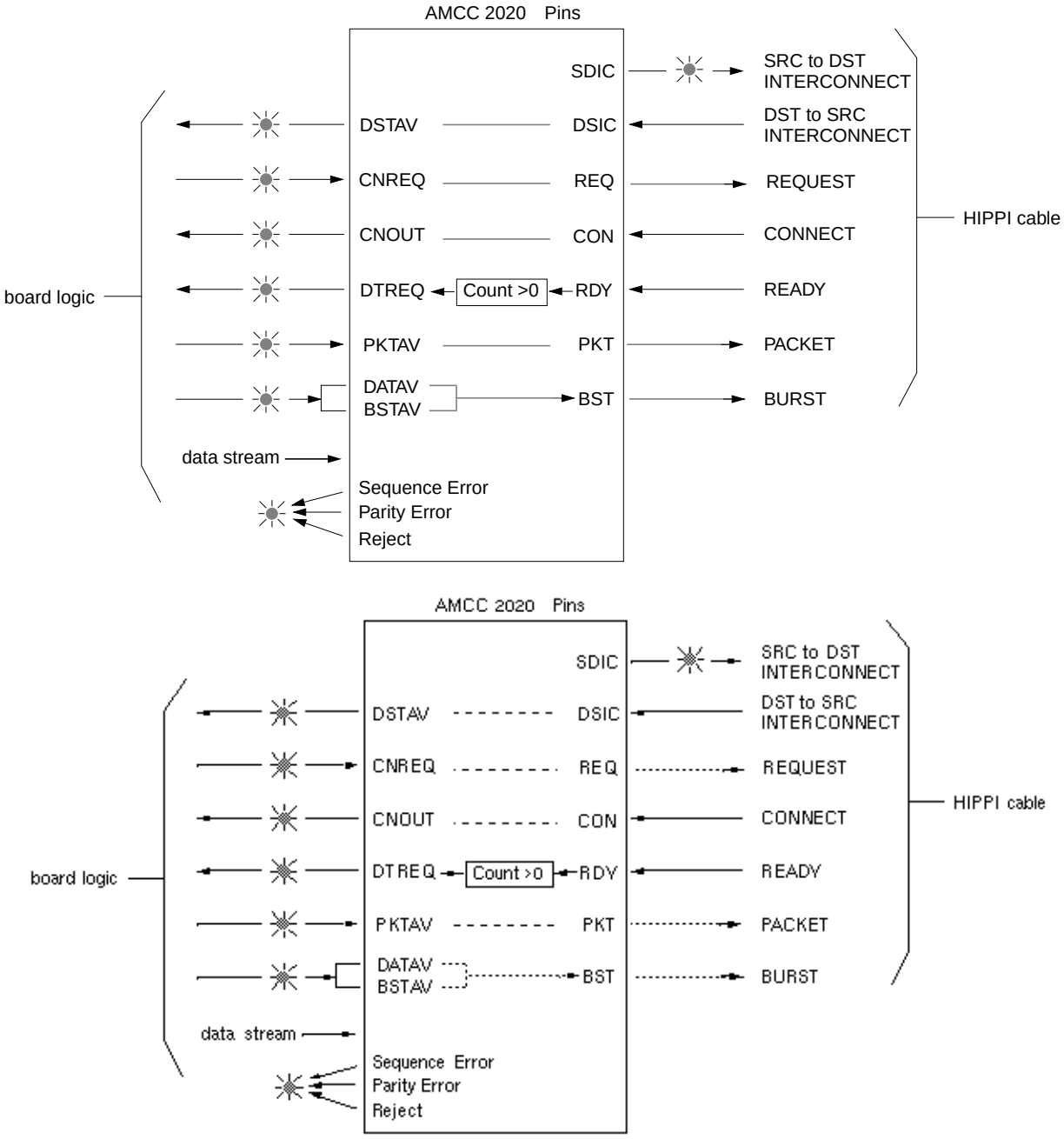
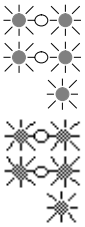


Figure 3-2 Signals That Control Source LEDs

3.6 Indications of Normal Operation

The LED combinations described in this section occur during normal operation.

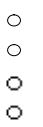
3.6.1 General



Green (blinking)
Yellow (blinking)
Red clocks (steadily on)

Green (blinking)
Yellow (blinking)
Red clocks (steadily on)

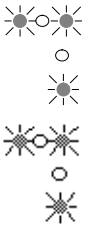
The board has not been initialized yet. This LED behavior is normal after a system reset and until the UNIX initialization scripts run to completion.



Green (off)
Yellow

Green (off)
Yellow

For a very short time during startup, both LEDs are off while new firmware is downloaded onto the board.

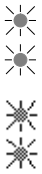


Green (blinking)
Yellow
Red clocks

Green (blinking)
Yellow
Red clocks

The board has been initialized successfully.

3.6.2 Destination Channel



Red Dst DSIC
Red Dst SRCAV

Red Dst DSIC
Red Dst SRCAV

The physical link is intact between the IRIS HIPPI board's destination and the switch or, if no switch exists, the other endpoint. Both ends of the physical link are online, not in test mode, and ready for action.

A source endpoint is attempting (requesting) to open a connection. The IRIS HIPPI board's firmware has not yet accepted the connection. This condition should be brief, unless you have configured the board to reject all connection requests; lengthy or frequent occurrences indicate a problem (as explained in Section 3.7, "Troubleshooting with LEDs").

A connection is open. Both endpoints are ready for a data transfer.

The firmware is telling the IRIS HIPPI board that the HIPPI subsystem is ready to accept data. This condition is not related to nor dependent on an open connection or a physical link.

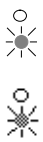
The source is sending a packet (that is, the **PACKET** line is currently asserted). Data are not being transmitted currently.

The IRIS HIPPI board is currently accepting a burst of data.

The IRIS HIPPI board's destination is not encountering any HIPPI errors on the incoming channel.

3.6.3 Source Channel

The physical link is intact between the IRIS HIPPI board's source and the switch or, if no switch exists, the other endpoint. Both ends of the physical link are online, not in test mode, and ready for action.



The IRIS HIPPI firmware is asking the board's source to open a connection. If the source channel's DSIC and DSTAV LEDs are on, the IRIS HIPPI board should be requesting the connection (that is, asserting the **REQUEST** line). The destination endpoint has not yet accepted the connection. This condition should be very short-lived. If the CNOUT LED fails to turn on, there is a problem, as explained in Section 3.7, "Troubleshooting with LEDs."

A connection is open. Both endpoints are ready for a data transfer.

The IRIS HIPPI board has at least one unused **READY** from the destination.

The source channel is ready to transmit. Data are not being transmitted currently.

Note: PKTAV normally remains on after a connection is terminated. This does not indicate a problem.

Red Src PKTAV
Red Src BSTAV

Red Src PKTAV
Red Src BSTAV

The IRIS HIPPI board is currently transmitting a burst of data.

Red Src ERROR

Red Src ERROR

The IRIS HIPPI board's source is not encountering any HIPPI errors on the outgoing channel.

Red Src ERROR

Red Src ERROR

Power has been turned on to the IRIS HIPPI board, and no connection has been setup as yet. When the first connection request is sent, this LED clears.

3.7 Troubleshooting with LEDs

The LED combinations described in this section indicate abnormal operation.

3.7.1 General

Green and yellow LEDs (off)
All red Dst and Src LEDs (off)

Green and yellow LEDs (off)
All red Dst and Src LEDs (off)

Indicates either no power to the IRIS HIPPI board or a malfunction of the IRIS HIPPI board.

Do the following steps to remedy this problem. After each step, check to see if the problem has been resolved before performing the next step.

1. Verify that the system has power.
2. If the system has power, verify that the IRIS HIPPI board is properly seated into its VMEBus slot and that the power modules for that VMEBus slot are functional. Alternatively, you might install the IRIS HIPPI board into a VME slot that is known to be functional in order to test the board.
3. Reboot the system to restart the IRIS HIPPI board.

If the problem persists, the IRIS HIPPI board may be dysfunctional. Contact the Silicon Graphics Technical Assistance Center.

There is power to the board, but the board has not been initialized. For the first few seconds during startup, this behavior is normal; however, when the UNIX initialization scripts complete, the yellow LED should turn off. If both LEDs continue to be on for more than 2 minutes, either the driver has not initialized the board or the board is dysfunctional.

Note: Do the following steps to remedy this problem. After each step, check to see if the problem has been resolved before performing the next step.

1. Using the command line shown below, verify that the operating system includes the IRIS HIPPI driver. If there are entries for `hippi`, the operating system has been built to include IRIS HIPPI. The board may be dysfunctional. Contact Silicon Graphics' Technical Assistance Center. If there are no entries for the IRIS HIPPI driver, continue to the next step.

   ```
   % grep hippi /usr/var/sysgen/master.c
   ```

2. Verify that the IRIS HIPPI software has been installed, using the *versions* command (as shown below). If the IRIS HIPPI software is not installed, follow the instructions in the *IRIS HIPPI Release Notes* to install it. If the software is installed, continue to the next step.

   ```
   % versions hippi
   ```

3. Use the *autoconfig* command to build a new operating system (IRIX kernel) that includes the IRIS HIPPI driver. Then, reboot the system to start using the new operating system.

   ```
   # /etc/autoconfig
   ....
   # /etc/reboot
   ```

If the problem persists, the IRIS HIPPI board may be dysfunctional. Contact the Silicon Graphics Technical Assistance Center.

There is power to the board, but the board has become dysfunctional. If the IRIS HIPPI board's firmware has failed, it attempts to determine the reason for the failure and to communicate the reason by blinking a code on the yellow LED. The code is a number of blinks. The code is repeated in the following manner: the code, a pause, the same code, a pause, and so on. The codes are summarized in Table 3-3.

Reboot the system to restart the IRIS HIPPI board.

If the problem persists, determine the reason for the failure from the code that the yellow LED is blinking, then, contact the Silicon Graphics Technical Assistance Center.

Table 3-3 Yellow LED Codes for Firmware Failure

Number of Yellow LED Blinks	Reason for Failure
1	Software failure
2	Bad interrupt
3	Source memory test failed
4	Destination memory test fail
5	Flash EEPROM checksum error
6	Debug interrupt
7	Trap 1 failure
8	Onboard CPU (29030) bus error failure

3.7.2 Destination

This section describes abnormal behavior for the destination channel.

```
Red Dst DSIC
Red Dst SRCAV
```

```
Red Dst DSIC
Red Dst SRCAV
```

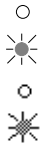
Indicates that the IRIS HIPPI board's destination channel is functional but that there is a malfunction somewhere between the board's destination AMCC 2021 component and the other end of the physical link.

Do the following steps to remedy this problem. After each step, check to see if the problem has been resolved before performing the next step.

1. Verify that the system at the other end (that is, a port at a switch or a network interface controller) is functional and online.
2. Use the *hiptest* utility and a loopback link to verify that this destination channel can receive data. (This procedure is documented in the *IRIS HIPPI Administrator's Guide*.) Alternatively, connect the destination channel to a different known-to-be-functional source endpoint. When the link to a functional source is installed, the SRCAV should turn on.
3. If you are using another HIPPI source endpoint instead of the loopback link, verify that the source and destination cables are not swapped. The destination must be connected to a source (or OUT).

4. Along the entire physical link, verify that all the HIPPI cable connectors are firmly seated. Be sure to check the internal connections to the IRIS HIPPI board as well as the external connections at the I/O panel.
5. Attach the external HIPPI cable directly to the IRIS HIPPI board. Disconnect the HIPPI cable from the destination connector on the I/O panel, open the I/O panel, disconnect the internal cable to the IRIS HIPPI board's connector, and connect the external cable directly to the IRIS HIPPI board's destination connector.
6. One by one, replace each of the cables between the IRIS HIPPI board's destination connector and the source on the other end of the physical link. Use cables that are known to be functional.

If the problem persists, the IRIS HIPPI board may be dysfunctional. Contact the Silicon Graphics Technical Assistance Center.



Indicates that the physical link and the system at the other end of the physical link are functional, but the IRIS HIPPI board has a malfunction. The problem may be as simple as the DSIC or SRCAV LED being broken, but it is also possible that the IRIS HIPPI board is dysfunctional.

Do the following steps to remedy this problem. After each step, check to see if the problem has been resolved before performing the next step:

1. At the other end (the source) of the physical link, check if the incoming Destination-to-Source **INTERCONNECT** signal is observed (asserted). If it is, the IRIS HIPPI board's DSIC LED is erroneously off.
2. At the other end (the source) of the physical link, check if the system is asserting its Source-to-Destination **INTERCONNECT** signal. If it is not, the IRIS HIPPI board's SRCAV LED is erroneously on.
3. Use *hinv* to verify that the IRIS HIPPI board has been located during startup. If the board is not listed, it is possible that the FMezz card, the IRIS HIPPI board, or the FCI cable is loose or dysfunctional.
4. Verify that the FCI cable between the FMezz board and the IRIS HIPPI board is firmly seated at both of its connectors.
5. Replace the FCI cable with a cable that is known to be functional.
6. Reboot the system to restart the board.
7. Shutdown the system and reinstall the IRIS HIPPI product (FMezz board and IRIS HIPPI board), taking extra precautions to seat the boards firmly into their connectors/backplanes. (Alternately, attach the IRIS HIPPI board's FCI cable to a different FMezz board, then reboot.)

Contact the Silicon Graphics Technical Assistance Center.

A source endpoint is attempting (requesting) to open a connection and the IRIS HIPPI board's firmware is not accepting the connection. The IRIS HIPPI board may be configured to reject all connection requests, or it may be dysfunctional.

Do the following to remedy this problem. If the problem persists, contact the Silicon Graphics Technical Assistance Center.

- Use the *hipcntl* command to configure the board to accept incoming connection requests:

  # **hipcntl accept**

Indicates a malfunction of the board's firmware or hardware.

Reboot the system to download new firmware. If the problem persists, contact the Silicon Graphics Technical Assistance Center.

3.7.3 Source

This section describes abnormal behavior for the source channel.

Indicates that the IRIS HIPPI source channel is functional but that there is a malfunction somewhere between the board's AMCC 2020 component and the other end of the physical link.

Do the following steps to remedy this problem. After each step, check to see if the problem has been resolved before performing the next step.

1. Verify that the system at the other end (that is, a port at a switch or a network interface controller) is functional and online.
2. Use the *hiptest* utility and a loopback link to verify that this source channel can send data. (This procedure is documented in the *IRIS HIPPI Administrator's Guide*.) Alternatively, connect the source channel to a different known-to-be-functional destination endpoint. When the link to a functional destination is installed, the DSTAV should turn on.
3. If you are using another HIPPI destination endpoint instead of the loopback link, verify that the source and destination cables are not swapped. The source must be connected to a destination (or IN).
4. Along the entire physical link, verify that all the HIPPI cable connectors are firmly seated. Be sure to check the internal connections to the IRIS HIPPI board as well as the external connections at the I/O panel.
5. Attach the external HIPPI cable directly to the IRIS HIPPI board. Disconnect the HIPPI cable from the source connector on the I/O panel, open the I/O panel, disconnect the internal cable to the IRIS HIPPI board's connector, and connect the external cable directly to the IRIS HIPPI board's source connector.
6. One by one, replace each of the cables between the IRIS HIPPI board's source connector and the destination on the other end of the physical link. Use cables that are known to be functional.

If the problem persists, contact the Silicon Graphics Technical Assistance Center.

Indicates that the physical link and the system at the other end of the physical link are functional, but the IRIS HIPPI board has a malfunction. The problem may be as simple as the SDIC or DSTAV LED being broken, but it is also possible that the IRIS HIPPI board is dysfunctional.

Do the following steps to remedy this problem. After each step, check to see if the problem has been resolved before performing the next step.

1. At the other end of the physical link (the destination), check if the incoming Source-to-Destination **INTERCONNECT** signal is observed (asserted). If it is, the IRIS HIPPI board's SDIC LED is erroneously off.
2. At the other end of the physical link (the destination), check if the system is asserting its Destination-to-Source **INTERCONNECT** signal. If it is not, the IRIS HIPPI board's DSTAV LED is erroneously on.
3. Use *hinv* to verify that the IRIS HIPPI board has been located during startup. If the board is not listed, it is possible that the FMezz card, the IRIS HIPPI board, or the FCI cable is loose or dysfunctional.
4. Verify that the FCI cable between the FMezz board and the IRIS HIPPI board is firmly seated at both of its connectors.

5. Replace the FCI cable with a cable that is known to be functional.
6. Reboot the system to restart the board.
7. Shutdown the system and reinstall the IRIS HIPPI product (FMezz board and IRIS HIPPI board), taking extra precautions to seat the boards firmly into their connectors / backplanes. (Alternately, attach the IRIS HIPPI board's FCI cable to a different FMezz board, then reboot.)

If the problem persists, contact the Silicon Graphics Technical Assistance Center.

Appendix A

Summary of Installation

This appendix contains a summary of the IRIS HIPPI installation for the different platforms.

A.1 Hardware Configuration Summary

Table A-1 HIPPI Hardware Configurations for Various Platforms

Platform	Maximum HIPPI Boards[a]	Maximum IO4 Boards
Challenge L Deskside	2	3
Challenge XL Rackmount	4	6
Onyx Deskside	1	1
Onyx Rackmount	4	4

a. In some situations, it is possible to install more IRIS HIPPI boards and IO4 boards. Contact the SGI sales respresentative for more details.

A.2 IRIS HIPPI Board

Table A-2 IRIS HIPPI Board Power Requirements

Average	75 watts of power (drawn from its VMEBus slot)
Maximum	5 volts at 15 amps, and 12 volts at 1.5 amps

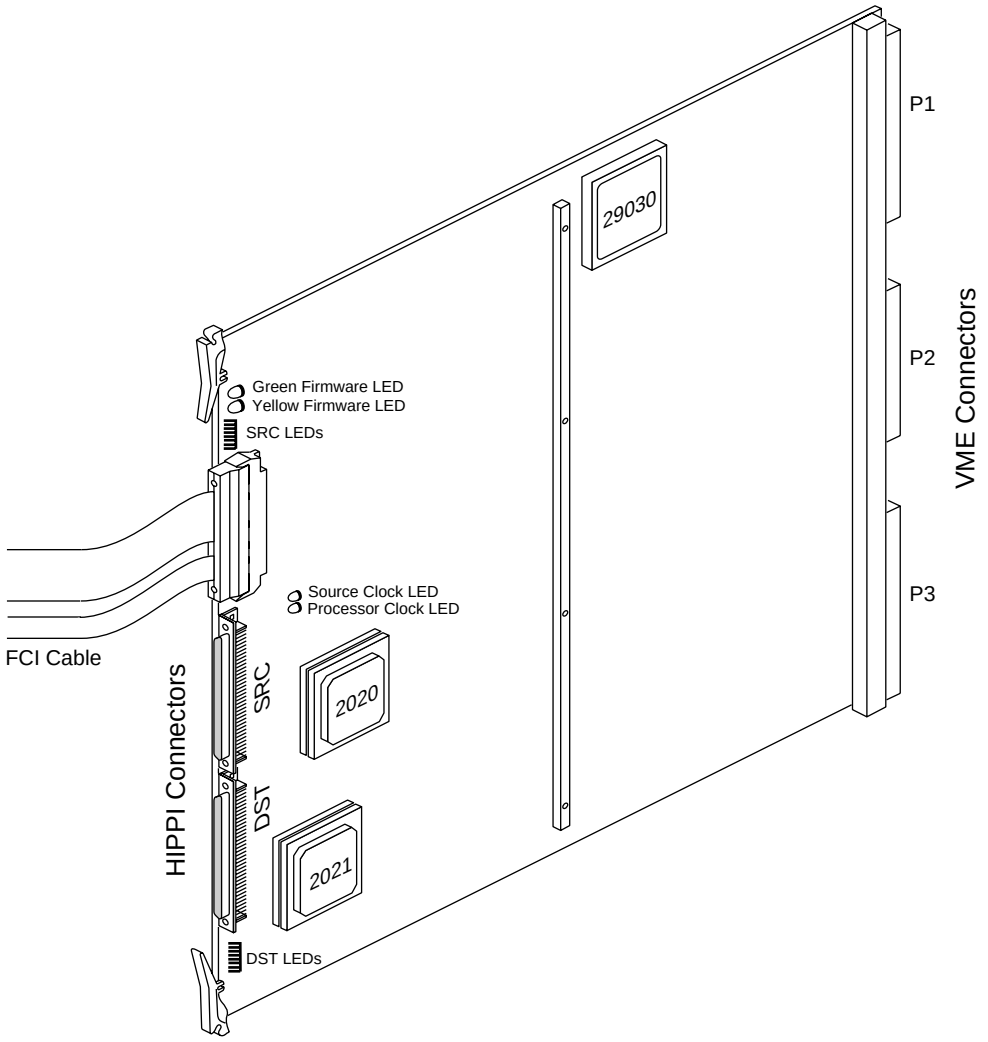


Figure A-1 IRIS HIPPI Board

A.3 Slot Requirements

Table A-3 Slots for IRIS HIPPI Installation in CHALLENGE Deskside System

Slots Required	Slots That Can Be Used
Mezzanine slot	Upper or lower mezzanine slot on an IO4 board in slot 5, 4, or 3
VMEBus slot	Slot 7, 8, 9, 10, or 11

Table A-4 Slots for IRIS HIPPI Installation in CHALLENGE XL Rackmount System

Slots Required	Slots That Can Be Used
Mezzanine slot	Upper or lower mezzanine slot on an IO4 board in slot 15, 13, 11, 9, 7, or 5
VMEBus slot	Slot 17, 18, 19, 20, or 21 in card cage 2; Sor any of slots 2-21 in card cage 3

Table A-5 Slots for IRIS HIPPI Installation in Onyx Deskside System

Slots Required	Slots That Can Be Used
Mezzanine slot	Upper or lower mezzanine slot on IO4 board in slot 3
VMEBus slot	Slot 5, 6, or 7

Table A-6 Slots for IRIS HIPPI Installation in Onyx Rackmount System

Slots Required	Slots That Can Be Used
Mezzanine slot	Upper or lower mezzanine slot on an IO4 board in slot 11, 9, 7, or 5
VMEBus slot	Slot 13, 14, or 15 in card cage 2; or slot 2, 3, 4, 12, 13, or 14 in card cage 3

A.4 Illustrations of Slot Locations

figs/chal.dsk.slots.ai 100%

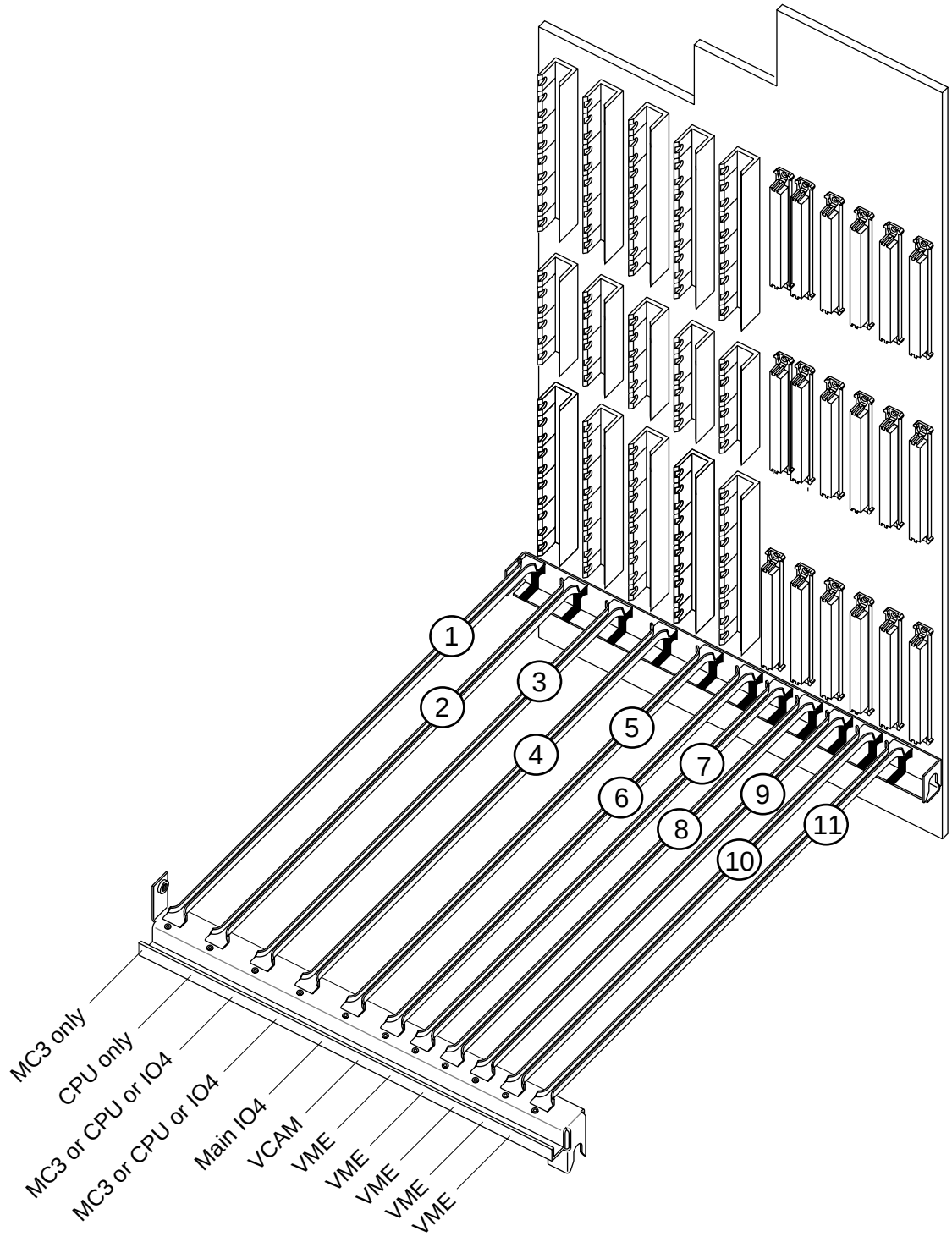


Figure A-2 CHALLENGE L Deskside Slots

figs/chal.rkmt.allslots.ai 100%

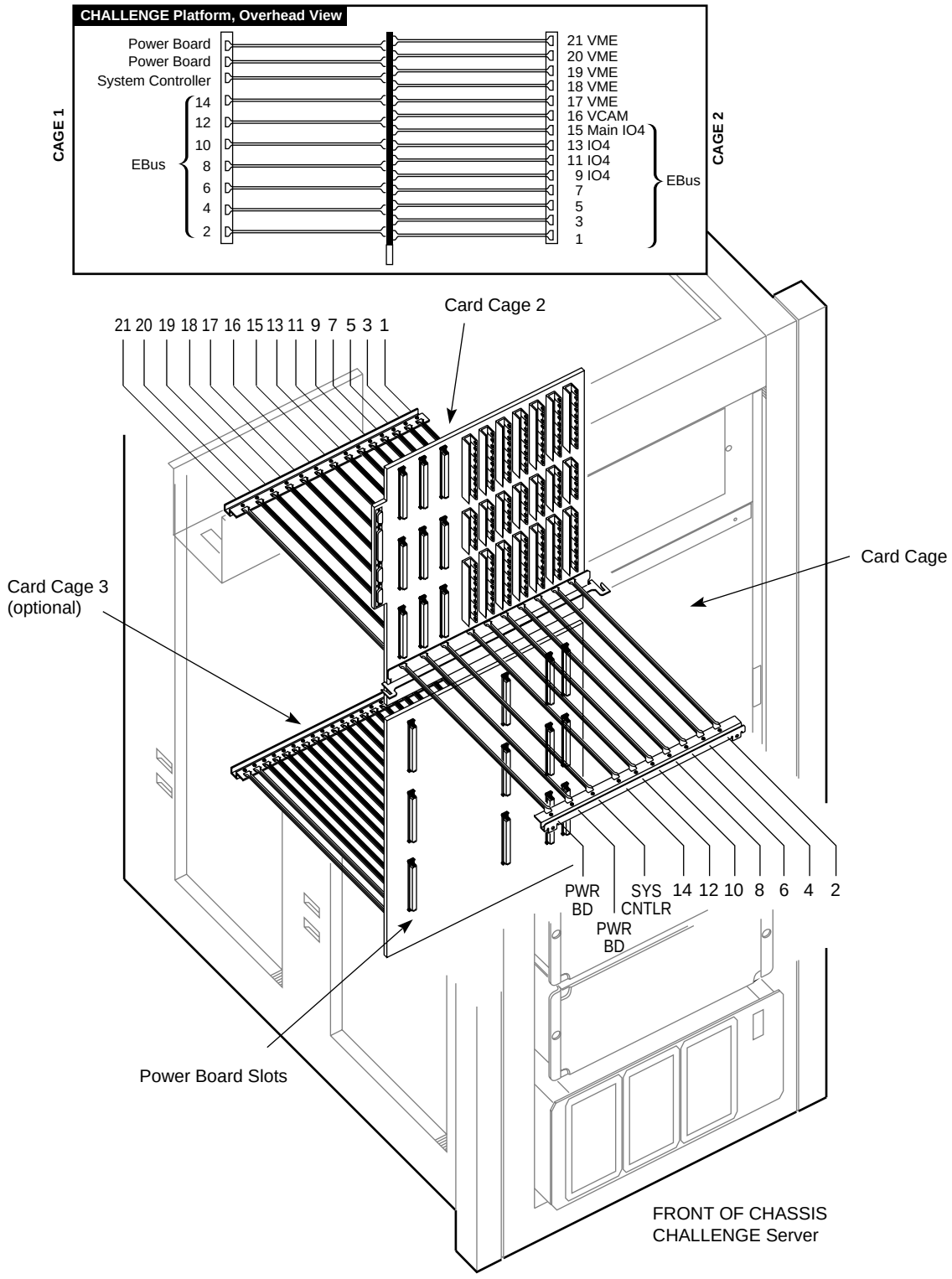


Figure A-3 CHALLENGE XL Rackmount Card Cages 1 and 2 Slots

figs/chal.cc3slots.ai 95%

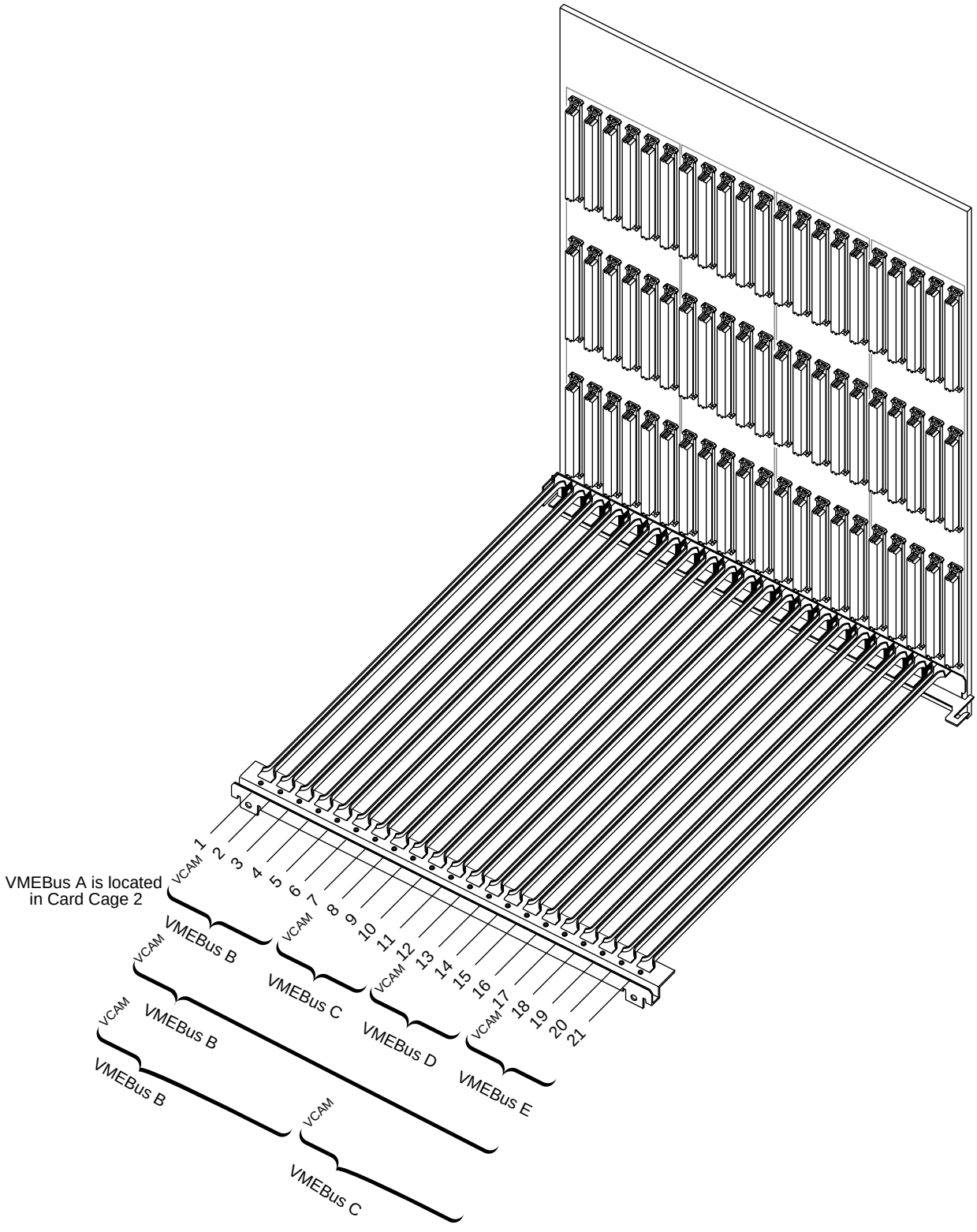


Figure A-4 CHALLENGE XL Rackmount Card Cage 3 Slots

figs/onyx.dsk.slots.ai 100%

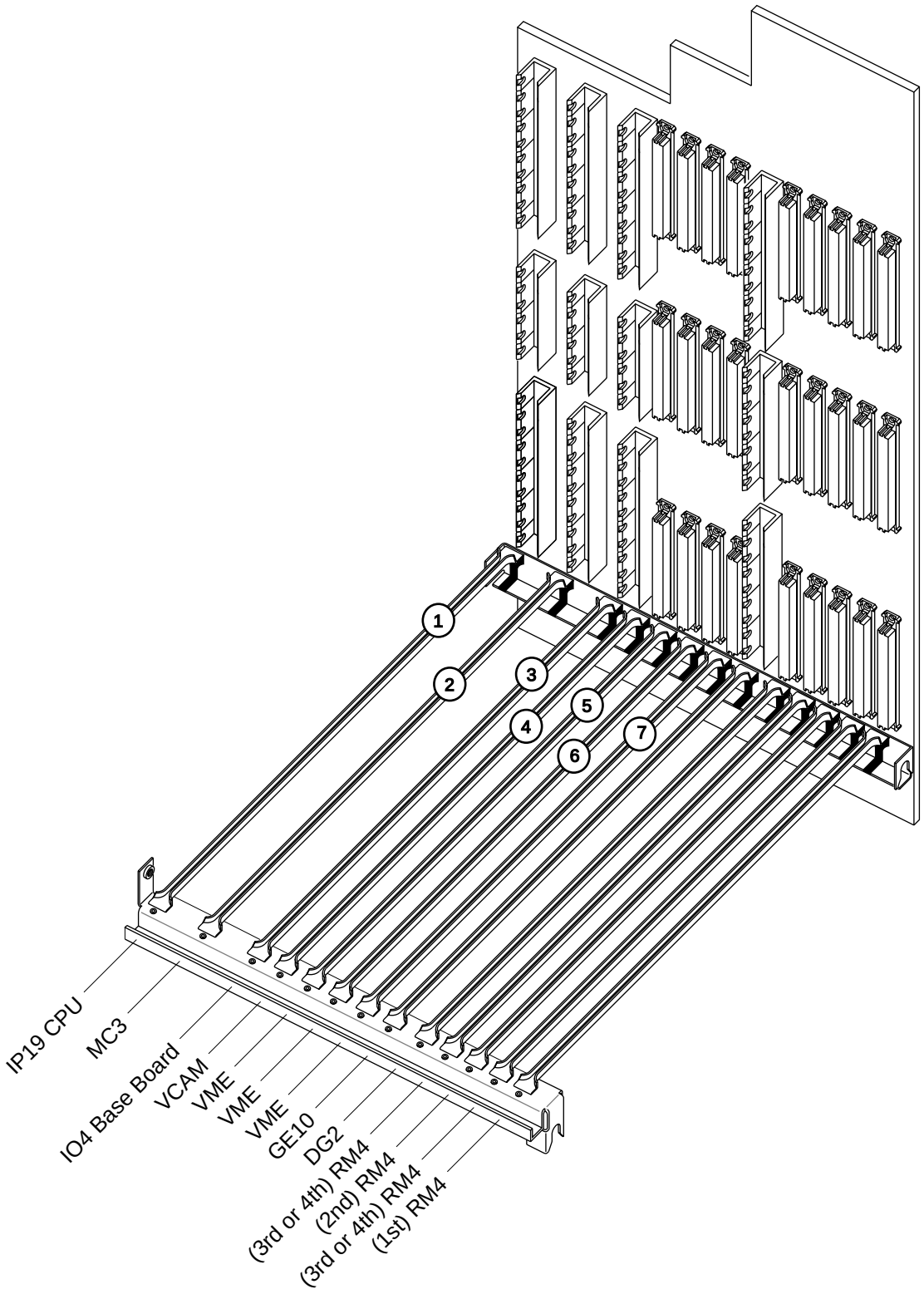


Figure A-5 Onyx Deskside Card Cage Slots

figs/onyx.rkmt.allslots.ai 100%

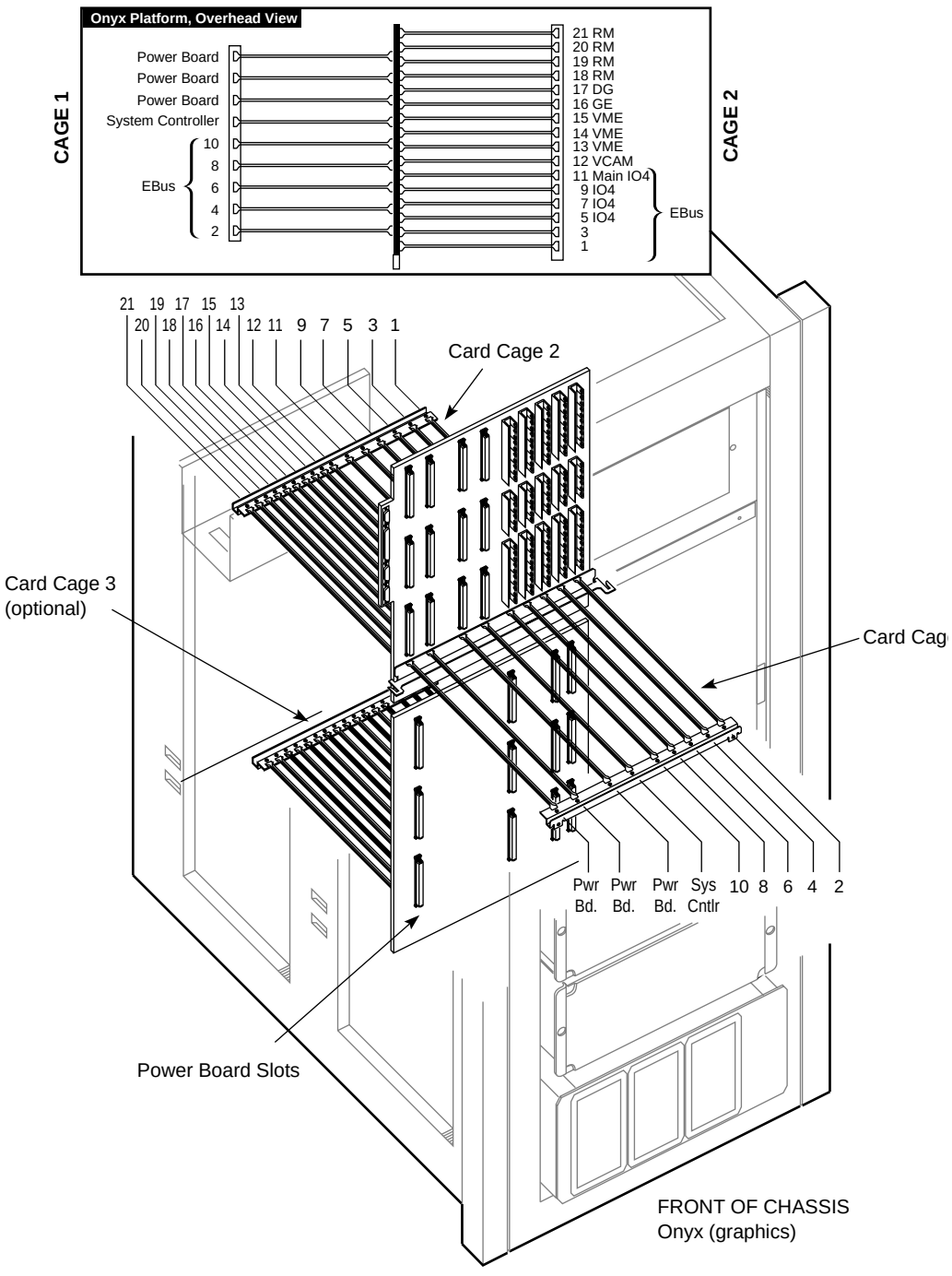


Figure A-6 Onyx Rackmount Card Cages 1 and 2 Slots

figs/onyx.cc3slots.ai 100%

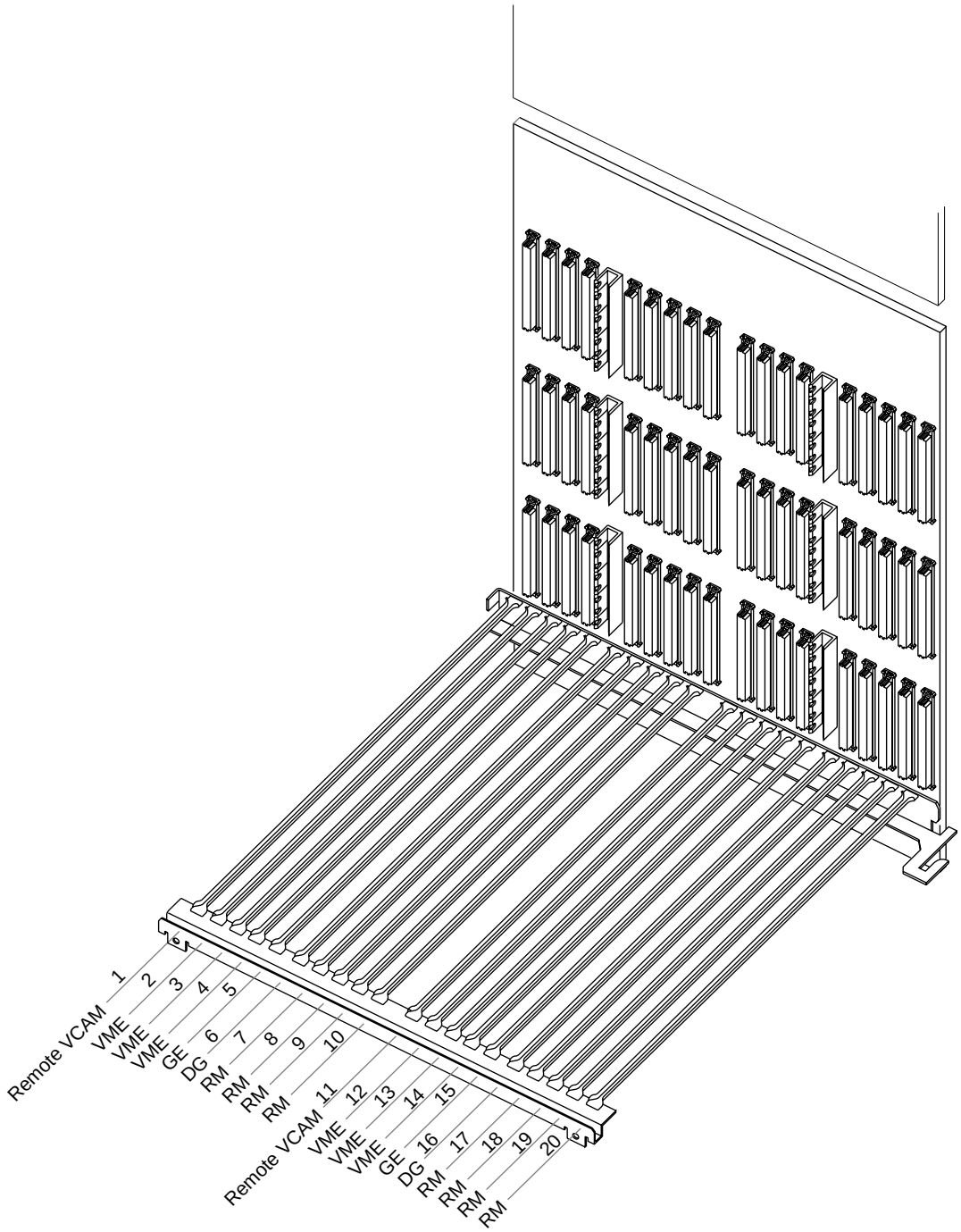


Figure A-7 Onyx Rackmount Card Cage 3 Slots

A.5 Error Messages

This section lists some of the error messages for which SSE troubleshooting procedures are recommended. (A more complete list of error messages is provided in the *IRIS HIPPI Administrator's Guide*.)

A.5.1 IRIX Messages Indicative of IRIS HIPPI Problems

Chapter 3The standard IRIX messages described in this section are displayed on the System Controller display panel located on the front of the CHALLENGE or Onyx chassis. These messages are not unique to IRIS HIPPI and may be caused by other system components.

`POKB`

Open the card cage I/O panel(s) and look for a board with a red LED. If the red LED occurs on an FMezz board to which an IRIS HIPPI board is attached (via the FCI cable), perform the following steps:

1. Shut down the system and turn the power off.
2. Disconnect the FCI cable.
3. Restart the system.
4. If the error message is displayed and the LED on the FMezz board is red again, the FMezz board is dysfunctional. Install a new FMezz board or connect the IRIS HIPPI's FCI cable to another installed FMezz board.

   If the LED on the FMezz board is green, the problem is with the IRIS HIPPI board. Follow the instructions in Chapter 3 to troubleshoot the IRIS HIPPI board, using its LEDs.

A.5.2 IRIS HIPPI Error Messages That Indicate Troubleshooting Is Required

The IRIS HIPPI error messages in this section indicate problems that only an SSE can troubleshoot and, in some cases, repair. For error messages that do not appear here, refer to the instructions in the *IRIS HIPPI Administrator's Guide*.

`hippi#: board asleep at` *iofile*`:`*line#* `with` *cmd_addr* `not` *cmd_addr* `after` *cmd_addr* `at` *line#*

The indicated IRIS HIPPI board (hippi#) controled by the indicated *iofile* is not responding to commands from the driver. The *line#* and *cmd_addr* variables indicate the expected and actual locations in the command queues. Use *hipcntl* to shut down then startup the IRIS HIPPI board.

If this does not resolve the problem, contact the Silicon Graphics Technical Assistance Center.

`hippi#: no board signature!`

While the startup software was attempting to initialize the host-to-board interface, the board's initialization firmware did not respond. This may indicate that the FLASH EEPROM does not contain firmware. Use the following command line to manually download new firmware, then restart the system:

```
%su
Password: thepassword
#/usr/etc/hipcntl hippi# download
#/etc/reboot
```

where `hippi#` identifies the problematic board (for example, hippi0, hippi1).

If this does not resolve the problem, contact the Silicon Graphics Technical Assistance Center.